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| dau_logo_BW | **EASTERN MEDITERRANEAN UNIVERSITY**  **MASTER OF TECHNOLOGY**  **COURSE POLICY SHEET** |  |

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| **Course Title** | Architecture and Hardware |
| **Course Code** | ITEC582 |
| **Type** | Full Time |
| **Semester** | Fall/Spring |
| **Category** | Area Elective |
| **Workload** | 150 Hours |
| **EMU Credit** | (3,0,0) 3 |
| **Prerequisite** | - |
| **Language** | English |
| **Level** | Graduate |
| **Teaching Format** | 3 Hours Lecture per week |
| **ECTS Credit** | 5 |
| **Course Web Site** | http://staff.emu.edu.tr/alperdoganalp/ |

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| **Instructor(s)** | Asst. Prof. Dr. Alper Doganalp | **Office Tel** | +90 392 6301600 |
| **E-mail** | alper.doganalp@emu.edu.tr | **Office No** | CT205 |

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| **Course Description** |
| The course provides the study of the structure, characteristics and operation of modern day computer systems including a basic background on the computers evolution, its design process and its internal characteristics which includes processor components, control unit architecture, memory organization and system organization. The concept of reduced instruction set computers (RISC), superscalar processors and superpipelining is explained in detail. The benefits of parallel processing and multicore processors are considered. |

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| **General Learning Outcomes** |
| On successful completion of this course students should be able to:   * Describe design principles for different instruction sets * Discuss different register organizations * Identify processor and register organizations * Describe instrcution pipelining and identify pipeline hazards * Discuss RISC/CISC processors * Explain superscalar execeution and superpipeline approaches * Identify symmetric multiprocessors and cache coherency protocols * Discuss Cluster and NUMA organizations * Describe multiple processor organizations * Discuss multicore organizations |

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| **Teaching Methodology / Classroom Procedures** |
| * The course has three hours of lectures in a week mainly held in the form of a seminar. * There is no lab works or tutorials. * There is one written midterm exam and one written final exam. * The exams are conducted as a written exam that may contain multiple choice, fill in the blanks, short answer and writing essay questions. * There is an individual term project.   + You should find a recent conference/journal paper (published in the last 5 years) related to Computer Architecture and Hardware.   + The selected paper should be sent as an e-mail to husnu.bayramoglu@emu.edu.tr and wait for the confirmation.   + Once the topic is confirmed, you can start studying the topic and prepare a written report.   + The printed report should be submitted before the announced deadline.   + Late submissions are not accepted.   + Project grade is out of 25%.   + The report should be between 3500-4000 words with the format provided in the report template on the web site.   + Turnitin plagiarism test must be obtained before submission.   + The plagiarism test result should be less than 20%.   + No reports are accepted for consideration with higher plagiarism test result.   + An account will be created for you to make the plagiarism test through Turnitin.   + The work done for the project should be presented.   + The duration of the presentation is about 15 minutes for each student.   + Presentation grade is out of 10%. * Class attendance is compulsory. * Lecture notes are available on the course web site. * Course related materials will be posted on the course web site. |

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| **Course Materials / Main References** |
| ***Text Book:***  William Stallings, Computer Organization and Architecture-Designing for Performance, Ninth Edition, Pearson Higher Education, 2013. ISBN 13: 978-0-13-293633-0 |

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| **Weekly Schedule / Summary of Topics** | |
| **Week 1** | ARM Data Types, Intel X86 Data Types |
| **Week 2** | Variable Length Instructions: PDP-11 Instruction Format, Intel x86 Instruction Format |
| **Week 3** | Register Organizations, Pipelining, Pipeline Hazards |
| **Week 4** | Instruction Execution Policies, RISC/CISC Processors |
| **Week 5** | Instruction Issue Policies |
| **Week 6** | Superscalar Execution, Superpipelining |
| **Weeks 7-8** | Midterm Examinations |
| **Weeks 9-10** | Symmetric Multiprocessors, Cache Coherency Protocols, Cluster Computer Architectures |
| **Week 11** | CC-NUMA (Cache Coherent Non-Uniform Memory Access) Organizations |
| **Week 12** | Multicore Organizations |
| **Week 13** | Presentations for Term Projects |
| **Week 14** | Presentations for Term Projects |
| **Week 15** | Presentations for Term Projects |
| **Weeks 16-18** | Final Examinations |

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| **Rules and Obligations** |
| * Each student can have only one make-up exam. One who misses an exam should provide a medical report within 3 days after the missed exam. * The make-up exam will be organized at the end of the term after the finals and will cover all the topics. * No make-up will be given for any quiz, project, presentation or assignment. * Once the grades are announced, the students have only one week to do objection about their grades. * It is the students’ responsibility to follow the announcement in the course web site. |

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| **Background Requirements** |
| * Students are expected to have a computer hardware background at minimum undergraduate level for registering the course. * Students who lack an official proof (such as undergraduate transcript) of the required academic background must acquire a written permission from the course instructor for registering the course. |

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| **Method of Assessment** | | | |
| Evaluation and Grading | **Term Project** | **Midterm Exam** | **Final Exam** |
| Percentage | 35 % | 30 % | 35 % |

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| **Grading Criteria \*** | | | | | | | | | | | |
| **A** | **A-** | **B+** | **B** | **B-** | **C+** | **C** | **C-** | **D+** | **D** | **D-** | **F** |
| 90 - 100 | 85 - 89 | 80 - 84 | 75 - 79 | 70 - 74 | 65 - 69 | 60 - 64 | 56 - 59 | 53 - 55 | 50 - 52 | 40 - 49 | 0 - 39 |

\* Letter grades will be decided upon after calculating the averages at the end of the semester and distribution of the averages will play a significant role in the evaluation of the letter grades.