CMPE224 – Digital Logic Systems

Department:
Computer Engineering

Program Name: Computer Engineering	**Program Code:** 25	
Course Number: CMPE224	**Credits:** 4 Cr	**Year/Semester:** 2018-2019 Spring

☒ Required Course ☐ Elective Course (click on and check the appropriate box)

Prerequisite(s):
CMPE223

Catalog Description:
This course presents the basic tools for the design of synchronous sequential circuits and covers methods and procedures suitable for a variety of digital design applications in computers, control systems, data communications, etc.. Concentration will be on widely-used design methods for synchronous sequential circuits together with their analysis and simulation in VHDL.

Course Web Page:
http://cmpe.emu.edu.tr/courses/cmpe224

Textbook(s):
S. Brown and Z. Vranesic, "*Fundamentals of Digital Logic with VHDL Design",* McGraw-Hill, Third Edition, 2009.

Indicative Basic Reading List :

- Richard S. Sandige. "***Digital Design Essentials***," Prentice-Hall 2002.
- John F. Wakerly, "*Digital Design: Principles and Practices"* Pearson Education, 2006.

Topics Covered and Class Schedule:
(4 hours of lectures per week)

Week 1	A review of synchronous sequential logic(SSL), flip-flops (FFs), VHDL implementation of FFs. Analysis of clocked sequential circuits, state transition tables/diagrams. Design of clocked sequential circuits, design procedure, state reduction and assignment, flip-flop excitation tables. Design procedure & case studies.
Week 2	Design of counters.
Week 3	Registers & shift registers
Week 4	Asyncronous ripple counters
Week 5	Synchronous counters & timing sequences. (First Quiz)
Week 6	Characteristics of ASM flow chart, timing considerations, Datapath implementation.
Week 7-8	ASM Controlpath implementation.
Weeks 9-10	**Mid-Term Examination**
Week 11	Introduction to computer architecture
Week 12	Processor architecture
Weeks 13	A generic processor architecture MARIE (Second Quiz)
Week 14	Programming and interfacing the generic processor
Week 15:	**Final Examination**

Laboratory Schedule:
(2 hours of laboratory per week)

Week 3 Introduction to Verilog HDL: principles of synchronous circuit design and simulation.
Week 4 Architectural design of synchronous sequential circuits.
Week 5 Behavioral design of synchronous sequential circuits
Week 6
Week 7
Week 11
Week 12

Course Learning Outcomes:

Students must be able to

1. know latches and flip-flops
2. know sychronous circuit operation
3. perform analysis of synchronous sequential circuits
4. understand fundamental design procedure for synchronous sequential circuits
5. carry out construction of initial state transition table / diagram
6. perform state reduction and state assignment
7. develop flip-flop excitations
8. perform design of registers and counters
9. make VHDL implementations: Structured design of synchronous sequential circuits
10. design shift registers and register data operations
11. perform design of synchronous and asynchronous counters
12. make VHDL implementations: Registers and counters
13. design algorithmic state machines (ASMs)
14. develop ASM charts and ASM blocks
15. make state assignment on ASMs
16. perform datapath design
17. perform controlpath design
18. make VHDL implementation of ASMs

	Method	**No**	**Percentage**
Assessment	Midterm Exam(s)	1	30%
	Lab Work(s)	7	10 %
	Quizzes	2	25 %
	Final Examination	1	35%

Contribution of Course to Criterion 5
Credit Hours for:

Mathematics & Basic Science : 0
Engineering Sciences and Design : 4
General Education : 0

Relationship of Course to Program Outcomes
The course has been designed to contribute to the following program outcomes:

(1) an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.
(6) an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions

GENERAL RULES:

- Attendance will be taken in all lectures. If your attendance is less than 50%, you will FAIL form the course irrespective of your all exam and lab-work scores.
- If you miss and exam, you can take a make up ONLY IF you submit a legal and official document (Medical report, court document, etc...) within THREE DAYS following the exam date. Late submission of documents will not be accepted and you will not be allowed to enter the make up exam in this case. **Makeup exams are organized by the Department (i.e. the date and rooms of makeup exams are announced by the Department).**
- You are allowed to take a makeup for ONLY ONE laboratory work. Ifyou miss another laboratory work without an official and acceptable document, you will get zero from that laboratory work. If you have three or more zeros from laboratory works, **the whole laboratory score will be zero**. If you fail from the lab-work, you will definitely fail from the course irrespective of other exam scores.
- There are absolutely no exemptions from the laboratory Work.
- Each laboratory work is organized as two hours explanation and demonstration in the laboratory and a weekly homework related to the demonstrated laboratory work IN ORDER TO COMPLETE A LABORATORY WORK, **YOU MUST ATTEND THE DEMONSTRATION** AND **YOU MUST SUBMIT THE WEEKLY HOMEWORK** ON TIME. If you don't complete TWO of the duties, you will get zero from the corresponding laboratory work. It is absolutely unacceptable to come the laboratories late, leaving the laboratories during demonstrations, and violating rules of laboratories. Late arrivals more than 10 minutes will be counted as "unattended" to laboaratory and you will not be allowed to enter the room.
- Cheating in exams and laboratory works is illegal and cause disciplinary investigation. You can cooperate with your friends, but your documents must be written in your words.
- You can check your Exam Papers within **ONE WEEK** following the announcement of examination scores and in **OFFICE HOURS ONLY.**

- You can reach all documents related to the course over web page: **http://cmpe.emu.edu.tr/courses/cmpe224 Visit this page regularly, all announcements made on this page are assumed to be known by all students taking the course and make you responsible to carry out the related duties.**

- It is very important to attend the lectures regularly. **All educational activities and announcements made in lectures are assumed to be known by all students taking the course**. The instructor is absolutely not responsible from any inconsistencies that may be caused due to your absences in lectures.

Prepared by: Assoc. Prof. Dr. Adnan Acan	**Date Prepared:** February 18, 2019