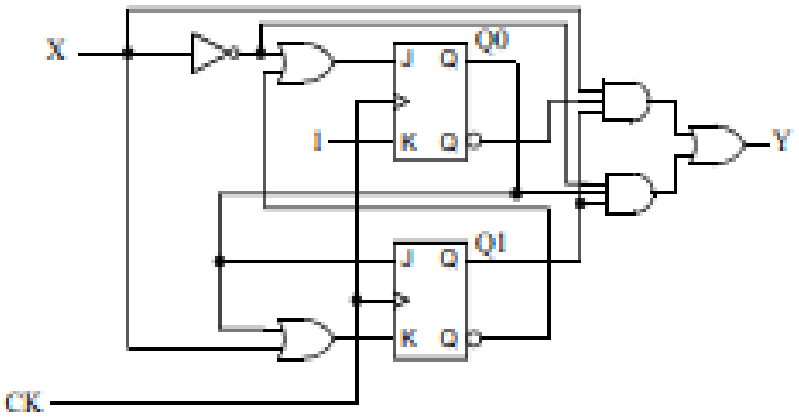
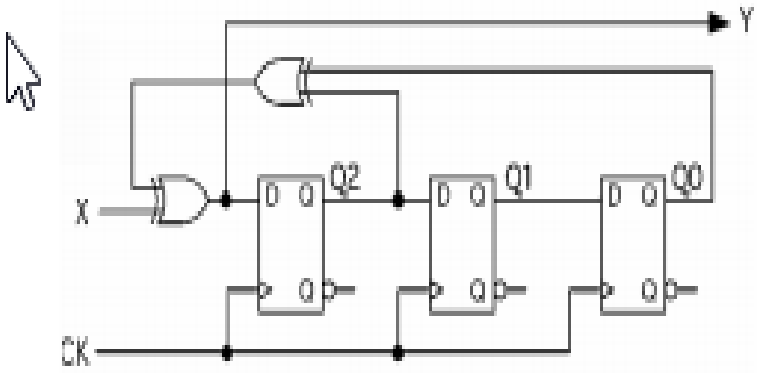
EASTERN MEDITERANEAN UNIVERSITY
COMPUTR ENGINEERING DEPARTMENT
CMPE224 DIGITAL LOGIC SYSTEMS
STUDY EXERCISES I

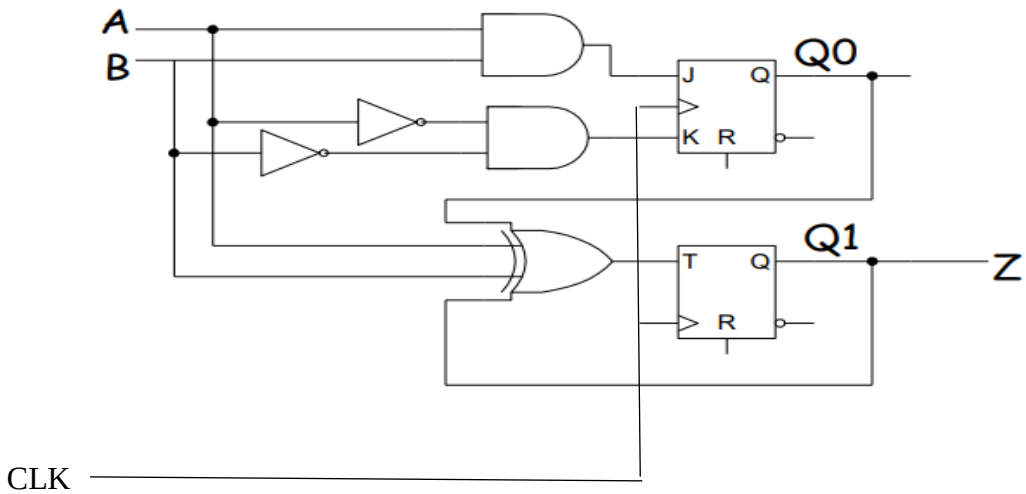
Q.1. Analyze the senkron sequential circuit given below and, draw the state transition table and the state transition diagram.



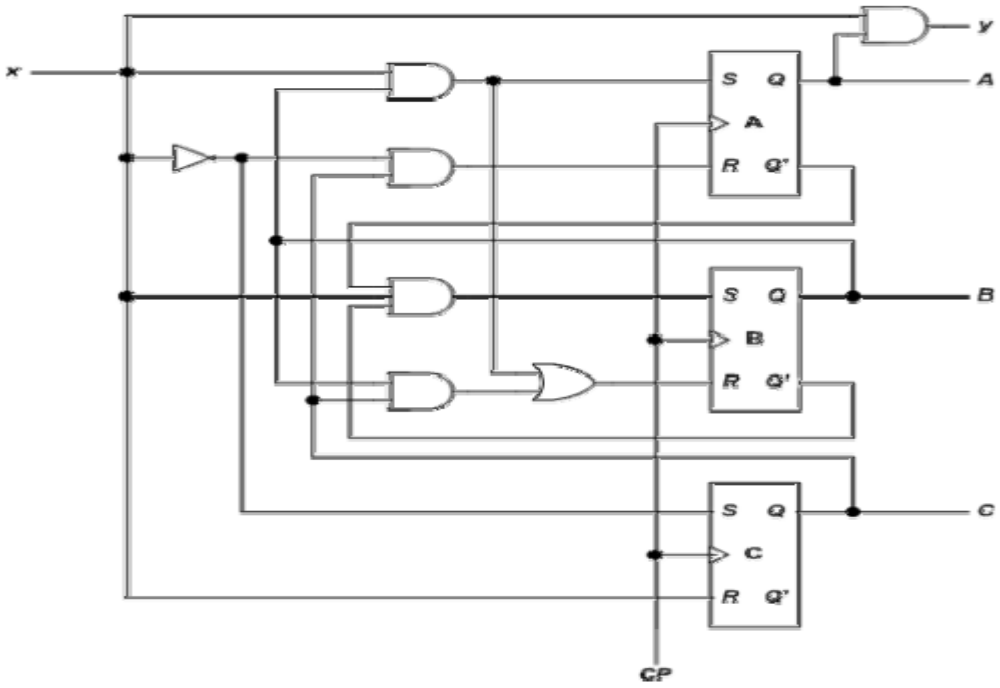
Q.2. Analyze the senkron sequential circuit given below and, draw the state transition table and the state transition diagram.



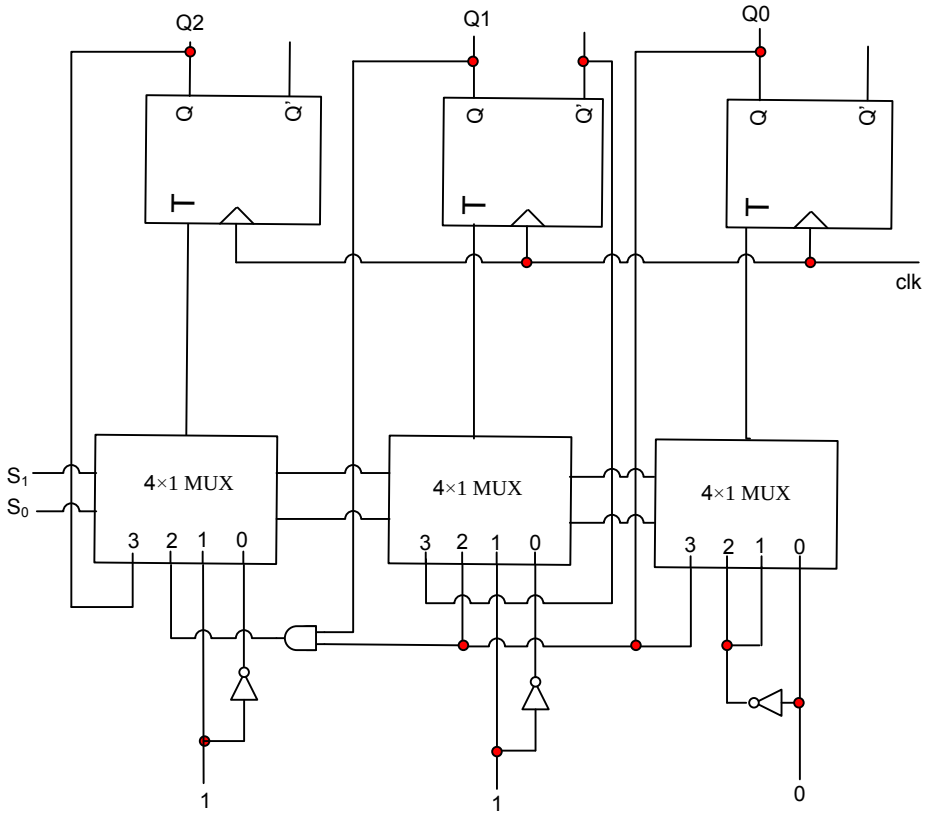
Q.3. Analyze the senkron sequential circuit given below and, draw the state transition table and the state transition diagram.



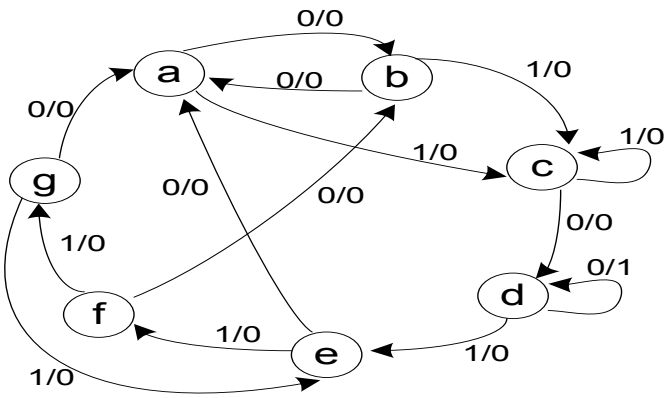
Q.4 Analyze the senkron sequential circuit given below and, draw the state transition table and the state transition diagram.



Q.5. Analyze the senkron sequential circuit given below and, draw the state transition table and the state transition diagram.



Q.6. Given the state transition diagram below:



a) Build the state transition table.
b) Minimize the number of states.
c) Make a state assignment, assign the FFs to state variables and, build the binary state transition table and the FF excitation table (one united table).
d) Obtain logic expressions and draw the circuit.

Q.7. A synchronous sequential circuit with one input **x** and one output **z** is required to work as follows: The output **z** will be **1** if and only if the last three consecutive bits on input **x** are equal to **0d0**, where **d** represents a don't care, and **z** will be **0** otherwise. Assume that the MSB arrives first and overlapping of the last three consecutive bits on **x** is allowed. Design this system using JK-FFs.

Q.8. You are required to design a synchronous sequential circuit with one input X and one output Y. The output Y will be equal to **1** if and only if ***the last three consecutive bits*** on X are **1dd** (**d** stays for don't care), Y=0 otherwise. Least signicant bit (LSB) arrives first (i.e. serial bits on X are arriving from left) and the three bit codes are overllaped. Design this system using D-FFs.

Q.9. You are asked to design a 2-bit counter with two control inputs A and B, that operates as follows: when AB=00, the counter stays in its corrent state (it keeps it current count), when AB=01, it *increments* its current count by 1, when AB=10, it *increments* the current count by 2 (count from 2 to 0, from 3 to 1), and when AB=11, it *decrements* the current count by 1. Design this counter using T flip-flops, show all design steps clearly and draw the designed circuit.

Q.10. Design a synchronous digital system, with two inputs X,Y and one ouput Z, which is required to work as follows: If the the last two consecutive bits on X and Y are complements of each other, then Z=1 and Z=0 otherwise. Assume that MSB arrives first and the two bit codeas are overlapped.

Example: X=1 1 **0 0** 0 1 0 **1 0** 1 **0 1** 1 0 1 **1 1 1** 1 **0 0** 0 0 ...

Y=0 1 **1 1** 0 0 0 **0 1** 1 **1 0** 1 0 1 **0 0 0** 1 **1 1** 0 1 ...

Z=0 0 0 1 0 0 0 0 1 0 0 1 0 0 0 0 1 1 0 0 1 0 0 ..

Design this system using a mixture of FFs.