EASTERN MEDITERRANEAN UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

CMPE224 DIGITAL LOGIC SYSTEMS

EXPERIMENTAL WOK #2

ARCHITECTURAL AND BEHAVIORAL DESIGN OF CLOCKED SEQUENTIAL CIRCUITS USING VERILOG HDL

OBJECTIVES:

This laboratory work aims to introduce a practical work on the design of synchronous sequential circuits from architectural and behavioral descriptions. The architectural description covers both the schematic and the software implementation of circuits designed through the conventional design procedure. The behavioral descriptions cover the implementation using Mealy and Moore type state transition diagrams.

Phase 1: Schematic-Entry

Assume that the circuit to be designed has one input X and one output Y such that Y=1 iff there are three or more consecutive ones over the input X; Y=0 otherwise.

1.1 Considering the Mealy type state transition diagram in class, design this clocked sequential circuit using JK-FFs. Then, input the schematic diagram of your design into VeriLog HDL and verify its correctness through waveform simulations (follow the steps explained in the first experimental work).

Phase 2: Implementing the design in Verilog HDL

Enter the VeriLog code of your design using Quartus Lite development suite. Compile and simulate your code to verify its correctness (follow the steps explained in the first experimental work).

Phase 3: Implementing the design using Mealy-type State Transition Diagram

Consider the Mealy-type state transition diagram described in lecture, the corresponding Verilog HDL code that implements the state-transition and output generation behavior of this digital system is given below:

```
module Seq_3Ones_Detect_Mealy(X,Clk,Y);
        input Clk,X;
        output Y;
        reg Y;

        reg [1:0] pstate,nstate;  // present and next state variables as registers
        parameter S0=2’b00, S0=2’b01, S0=2’b10, S0=2’b11; // state assignment

        always @(posedge Clk)
                case(pstate)
                        S0: if (x) begin nstate=S1; Y=0; end
                            else    begin nstate=S0; Y=0; end
                        S1: if (x) begin nstate=S2; Y=0; end
                            else    begin nstate=S0; Y=0; end
                        S2: if (x) begin nstate=S3; Y=1; end
                else    begin nstate=S0; Y=0; end
            S3: if (x) begin nstate=S3; Y=1; end
                else    begin nstate=S0; Y=0; end
        endcase
    // sequential logic for state transitions
        Pstate <= nstate;
endmodule
```

Write the above given code in VeriLog HDL environment and simulate it to verify its correctness.

Phase 4: Implementing the design using Moore-type State Transition Diagram

Consider the Moore-type state transition diagram described in lecture, the corresponding Verilog HDL code that implements the state-transition and output generation behavior of this digital system is given below:

```
module Seq_3Ones_Detect_Moore(X,Clk,Y);
    input Clk,X;
    output Y;

    reg [1:0] state;  // state variables as register
    parameter S0=2’b00, S0=2’b01, S0=2’b10, S0=2’b11; // state assignment

    always @(posedge Clk)
        case(state)
            S0: if (x) state <= S1;
                else   state <= S0;
            S1: if (x) state <= S2;
                else   state <= S0;
            S2: if (x) state <= S3;
                else   state <= S0;
            S3: if (x) state <= S3;
                else   state <= S0;
        endcase

    // define the output
        assign Y=(state == S3);
endmodule
```

Write the above given code in VeriLog HDL environment and simulate it to verify its correctness.

HOMEWORK #2 : (To be submitted at the beginning of the next laboratory work)

Design a clocked sequential circuit with one input X and one output Z for the detection of the 4-bit sequence 0110 on input line X. Output Z=1 when this sequence is detected, Z=0 otherwise. Overlapping of 4-bit codes are allowed. Assume that MSB arrives first.

i. Implement and simulate your design in VeriLog HDL environment the Mealy-type state transition diagram.
ii. Implement and simulate your design in VeriLog HDL environment the Moore-type state transition diagram.