Example:

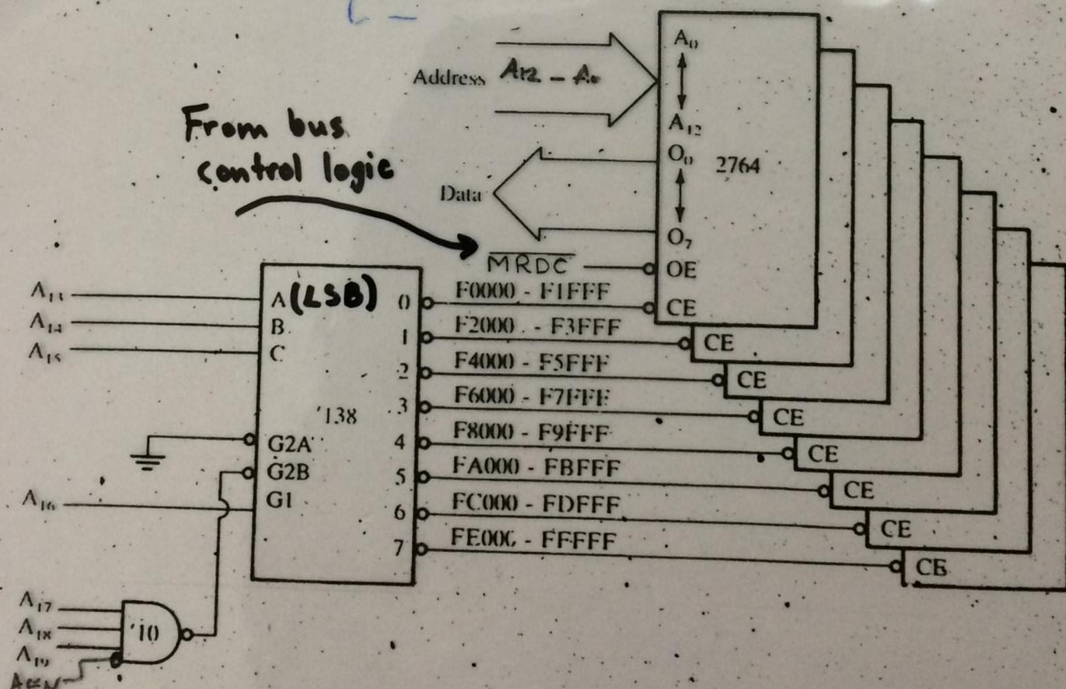
Eight 2764 (8K × 8) EPROMs are to be added to an 8088 microprocessor-based system in the address range F0000H-FFFFFH. Design a decoding circuit using a 74LS138 decoder.

in-chip addressing (A_{12} - A_0)

$2^{13} = 8K = 8192$ locations

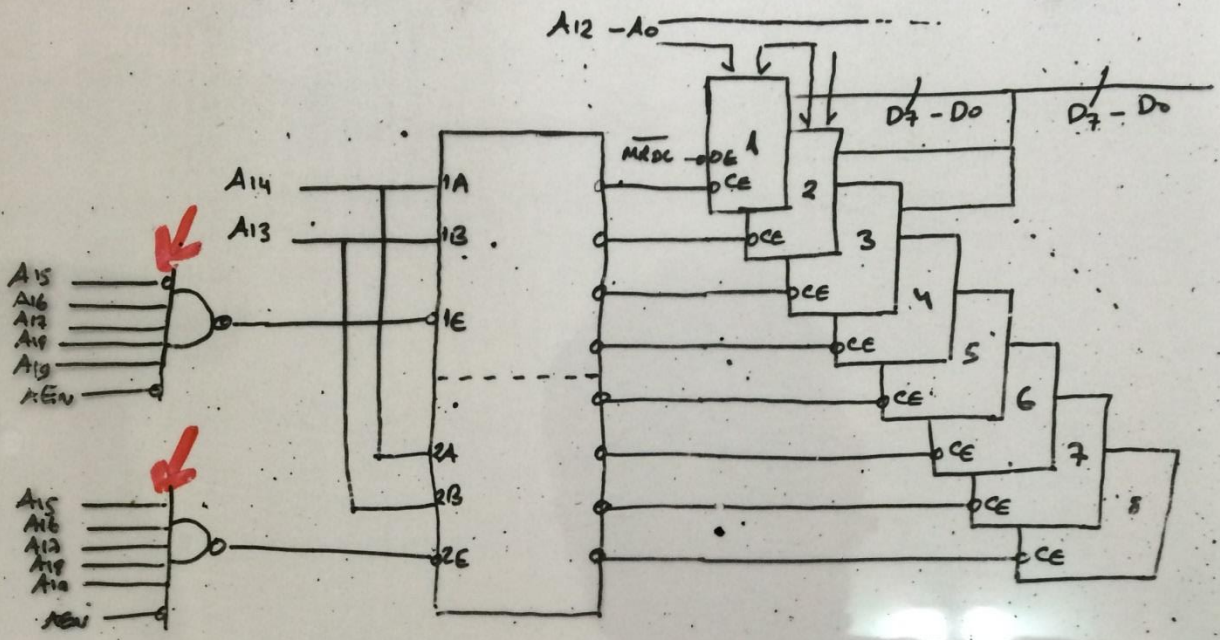
Chip 0	: 1111 0000 0000 0000 0000	= F0000H
	1111 0001 1111 1111 1111	= F1FFFH
Chip 1	: 1111 0010 0000 0000 0000	= F2000H
	1111 0011 1111 1111 1111	= F3FFFH
Chip 2	: 1111 0100 0000 0000 0000	= F4000H
	1111 0101 1111 1111 1111	= F5FFFH
Chip 3	: 1111 0110 0000 0000 0000	= F6000H
	1111 0111 1111 1111 1111	= F7FFFH
Chip 4	: 1111 1000 0000 0000 0000	= F8000H
	1111 1001 1111 1111 1111	= F9FFFH
Chip 5	: 1111 1010 0000 0000 0000	= FA000H
	1111 1011 1111 1111 1111	= FBFFFH
Chip 6	: 1111 1100 0000 0000 0000	= FC000H
	1111 1101 1111 1111 1111	= FDFFFH
Chip 7	: 1111 1110 0000 0000 0000	= FE000H
	1111 1111 1111 1111 1111	= FFFFFH

1FFFH = $(8191)_{10}$



A circuit that uses eight 2764 EPROMs for a 64K × 8 section of memory in an 8088 microprocessor-based system. The addresses selected in this circuit are F0000H–FFFFFH.

Q.1) 8 (8K×8) EPROMS in the address range: F0000-FFFFF using 74LS139

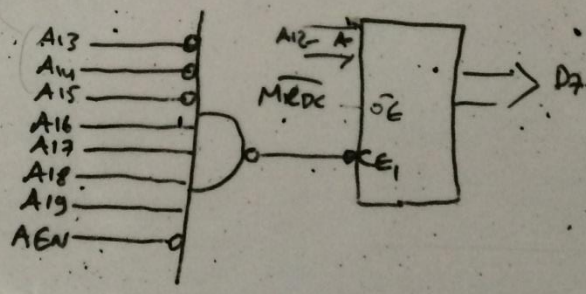


Q.2) 6 (8K×8) EPROMs and 1 (16K×8) EPROM in the address range. F0000 H - FFFFF H. using NAND gates.

EPROM1: F0000 — F1FFF

i.e 1111 0000 0000 0000 0000 ← in-chip addressing (A12-A0)
1111 0001 1111 1111 1111

⇒

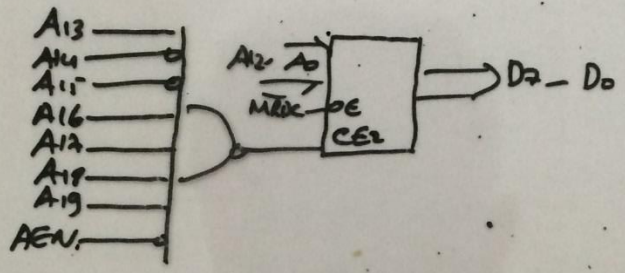


Similarly,

EPROM2: F2000 – F3FFF

i.e 1111 0010 0000 0000 0000
1111 0011 1111 1111 1111
in-chip addressing

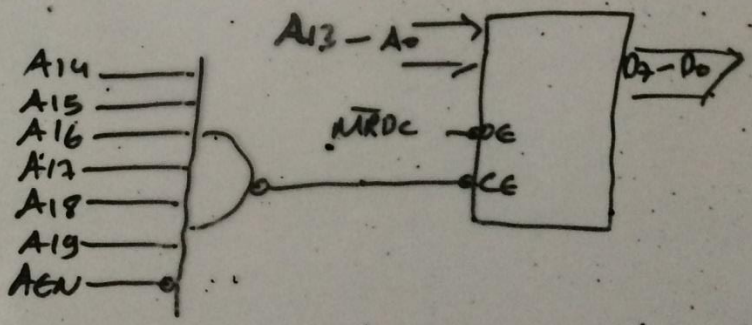
⇒



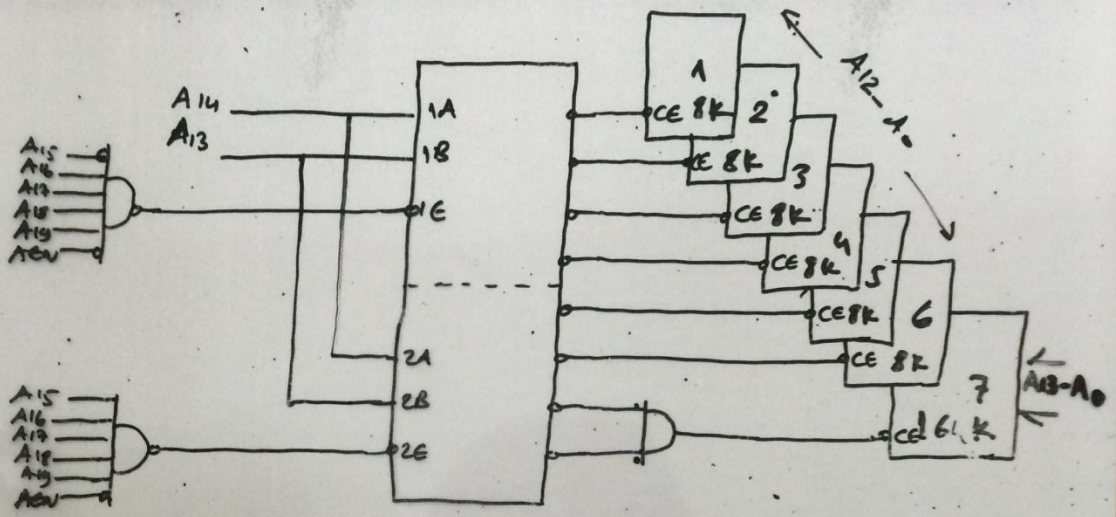
EPROM7: (16K) FC000 – FFFFF

i.e 1111 1100 0000 0000 0000
1111 1111 1111 1111 1111
in-chip addressing (A13 – A0)

⇒

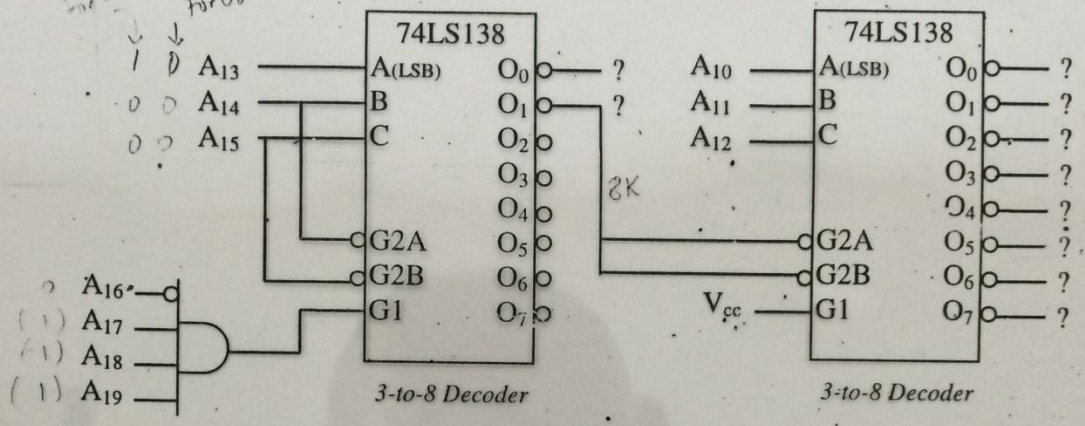


(8.4) Repeat Q.2 using 74LS 139 decoder



Q.1) [20 pts] $2^{20} = 1MB$

For an 80386 system working in real mode, the following address decoding circuit is given. (AEN is neglected).



a) [15 pts] What range of addresses (in H) correspond to each output of the decoders?

b) [5 pts] What is the total number of bytes in all ranges decoded by this circuit?

Answer: $2^{13} = 8K = 1FFF$

[A]

a) 1st Decoder outputs: $A_{19}\ A_{18}\ A_{17}\ A_{16}\ A_{15}\ A_{14}\ A_{13}\ A_{12}$ ..... A_0

For $O_0 \equiv$ 1 1 1 0 0 0 0 0 0000 0000 0000

1 1 1 0 0 0 0 1 1111 1111 1111 ≡ E0000-E1FFF = 8K

For $O_1 \equiv$ 1 1 1 0 0 0 1 0 0000 0000 0000

1 1 1 0 0 0 1 1 1111 1111 1111 ≡ E2000-E3FFF = 8K

2nd Decoder outputs: $A_{19}\ A_{18}\ A_{17}\ A_{16}\ A_{15}\ A_{14}\ A_{13}\ A_{12}\ A_{11}\ A_{10}$ ..... A_0

For $O_0 \equiv$ 1 1 1 0 0 0 1 0 0 0 0000 0000

1 1 1 0 0 0 1 0 0 0 1111 1111 ≡ E2000-E23FF = 1K

Similarly,

For $O_1 \equiv$ E2400-E27FF = 1K

For $O_2 \equiv$ E2800-E2BFF = 1K

For $O_3 \equiv$ E2C00-E2FFF = 1K

For $O_4 \equiv$ E3000-E33FF = 1K

For $O_5 \equiv$ E3400-E37FF = 1K

For $O_6 \equiv$ E3800-E3BFF = 1K

For $O_7 \equiv$ E3C00-E3FFF = 1K

b) 8K + 8K = 16K {same answer for **[B]**}

[B]

a) 1st Decoder outputs: For $O_0 \equiv$ 70000-71FFF = 8K; For $O_1 \equiv$ 72000-73FFF = 8K

2nd Decoder outputs: For $O_0 \equiv$ 72000-723FF = 1K; For $O_1 \equiv$ 72400-727FF = 1K

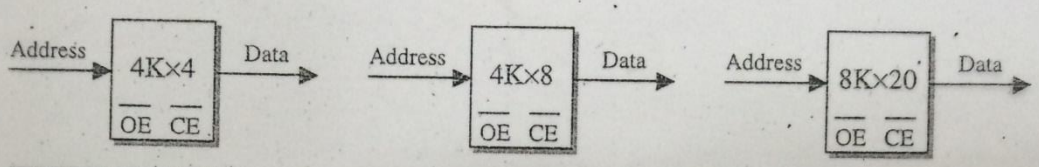
For $O_2 \equiv$ 72800-72BFF = 1K; For $O_3 \equiv$ 72C00-72FFF = 1K

For $O_4 \equiv$ 73000-733FF = 1K; For $O_5 \equiv$ 73400-737FF = 1K

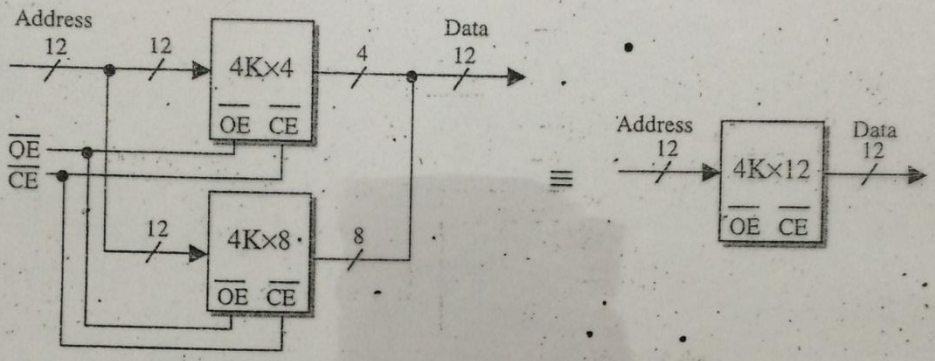
For $O_6 \equiv$ 73800-73BFF = 1K; For $O_7 \equiv$ 73C00-73FFF = 1K

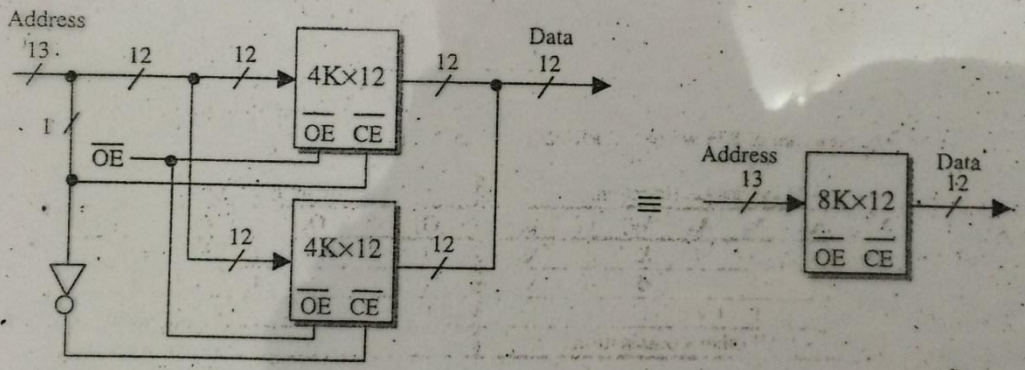
Q.3) [25pts]

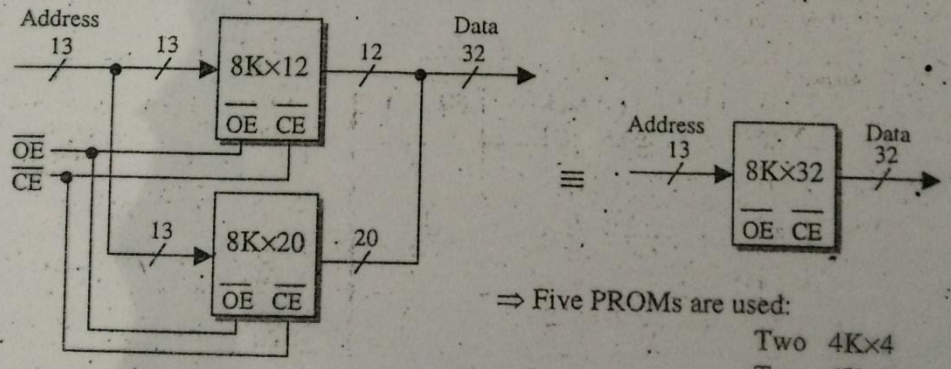
Using a **minimum** number of the PROM chips shown below, construct a 8K×32 bit PROM memory. (Show your design as block diagrams indicating the necessary connections of address, data and control signals).



Answer:







⇒ Five PROMs are used:

Two 4K×4
Two 4K×8
One 8K×20

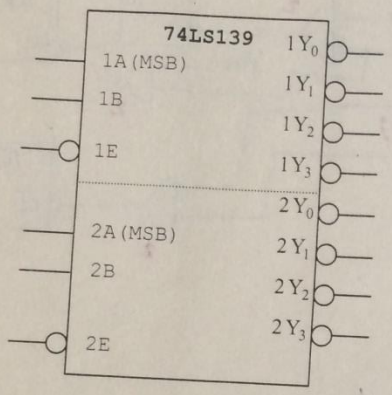
Q3) [30 points]

There is a need to add 56K byte of memory to an 80386 microprocessor based system (20-bit address bus and 8-bit data bus) in the address range A0000H-ADFFFH. The quantity of memory chips and the corresponding address ranges are as follows:

- 4 (8Kx8) RAM chips will be used to decode A0000H-A7FFFH
- 2 (4Kx8) RAM chips will be used to decode A8000H-A9FFFH
- 1 (16Kx8) RAM chip will be used to decode AA000H-ADFFFH

a) (16p)Design an address decoding circuit using a 74LS139 decoder. Show all connections and signals in detail.

b) (6)Determine the address range and its size in KB available in the memory map for any additional memory chip.



a)

(2)

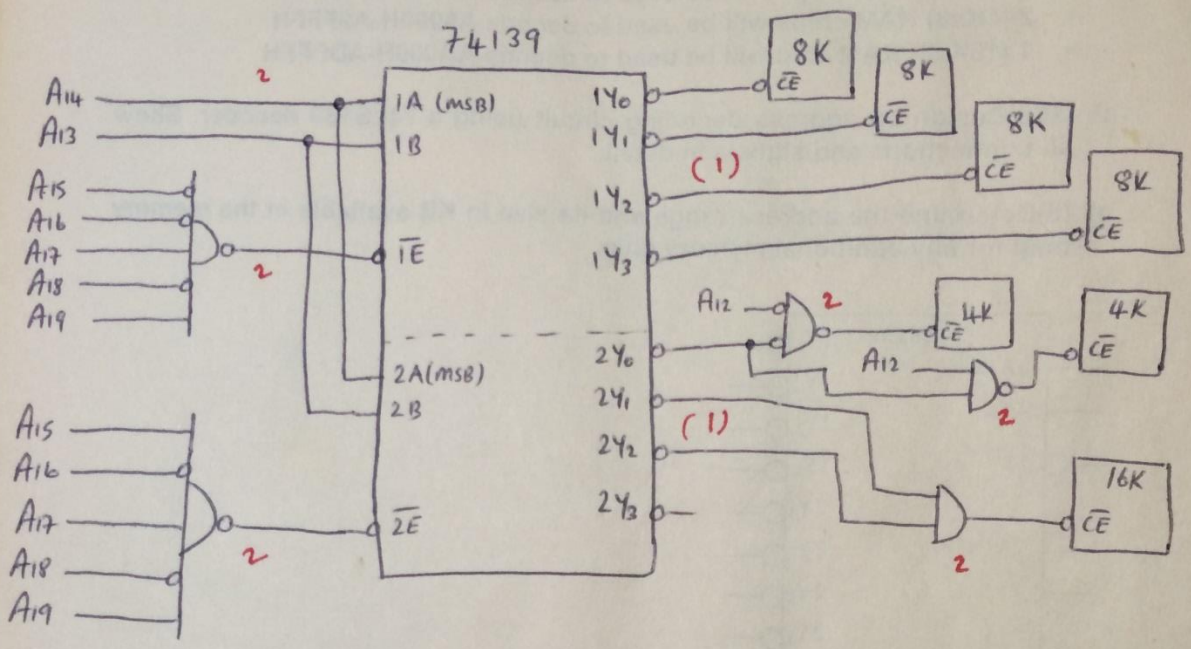
A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12} (in-chip)	A_{11}	A_{10}	...	A_0	
1	0	1	0	0	0	0	0	0			0	A0000 - A1FFF
1	0	1	0	0	0	0	1	1			1	
1	0	1	0	0	0	1	0	0			0	A2000 - A3FFF
1	0	1	0	0	0	1	1	1			1	
1	0	1	0	0	1	0	0	0			0	A4000 - A5FFF
1	0	1	0	0	1	0	1	1			1	
1	0	1	0	0	1	1	0	0			0	A6000 - A7FFF
1	0	1	0	0	1	1	1	1			1	
1	0	1	0	1	0	0	0	0	0		0	A8000 - A8FFF
1	0	1	0	1	0	0	0	1	1		1	
1	0	1	0	1	0	0	1	0	0		0	A9000 - A9FFF
1	0	1	0	1	0	0	1	1	1		1	
1	0	1	0	1	0	1	0	0	0		0	AA000 - ADFFF
1	0	1	0	1	1	0	1	1	1		1	

in-chip

in-chip

in-chip

Address Decoder



b) Available address ranges are

00000 - 9FFFF

AE000 - FFFFF

Total size of the available memory is 944KB.