eastern mediterranean university

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ID : *CMPE-224*

COMPUTER ENGINEERING DEPARTMENT
CMPE-224 DIGITAL LOGIC SYSTEMS **Friday 17/08/2001**

Q.1) [24 pts]
A set-dominant flip-flop has set (S) and reset (R) inputs. It differs from a conventional SR flip-flop in that when both S and R are equal to 1, the flip-flop is set.

a) Obtain the characteristic table of the set-dominant flip-flop.
b) Draw the state transition diagram of the set-dominant flip-flop.
c) Obtain the excitation table of the set-dominant flip-flop.
d) Implement the set-dominant flip-flop using a JK flip-flop and minimum number of gates.

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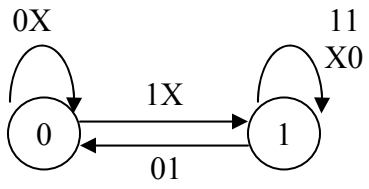
a)

S	R	Q(t+1)	
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	1	Set

b)



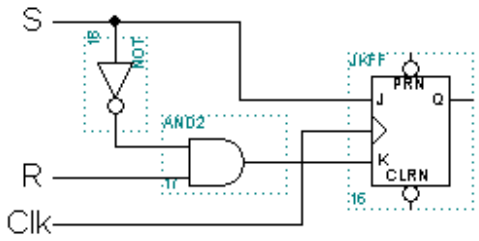
c)

Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	X
1	0	0	1
1	1	X	X

d)

S	R	Q(t)	Q(t+1)	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	1	1	X
1	1	1	1	X	0

Using K-map (you have to show this):
$J = S$, and $K = S' R$



Q.2) [24 pts]
A sequential circuit has one input ***X*** and one output ***Y***. The output ***Y*** is equal to 1 if and only if a 3-bit binary number formed by three consecutive bits on ***X*** is divisible by 3 (LSB is applied first). Otherwise, the output ***Y*** is equal to 0. The circuit returns to its initial state after checking the 3-bit binary number.

a) Draw your preliminary state transition diagram.
b) Find the reduced state table by applying state reduction.
c) Make near-optimal state assignments.

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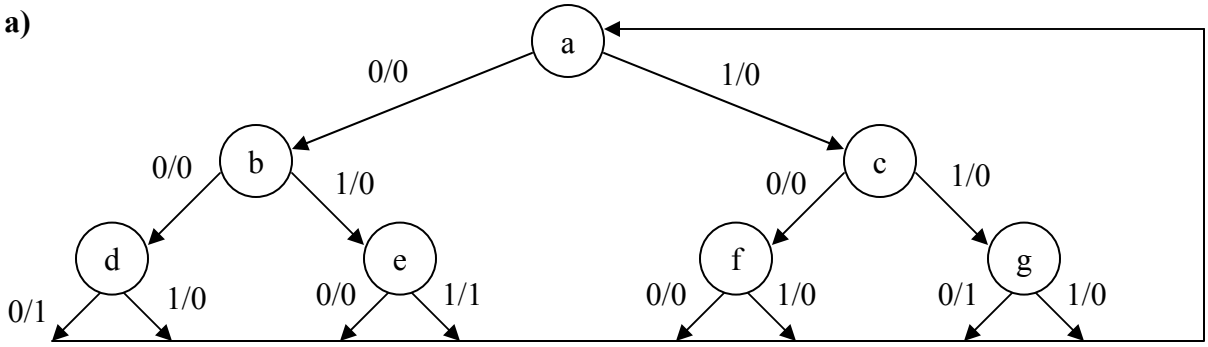
a)



b)

PS	NS		Output Y	
	X=0	X=1	X=0	X=1
a	b	c	0	0
b	d	e	0	0
c	f	g	0	0
d	a	a	1	0
e	a	a	0	1
f	a	a	0	0
g	a	a	1	0

P1 = (abcf) (dg) (e)
P2 = (af) (b) (c) (dg) (e)
P3 = (a) (f) (b) (c) (dg) (e)

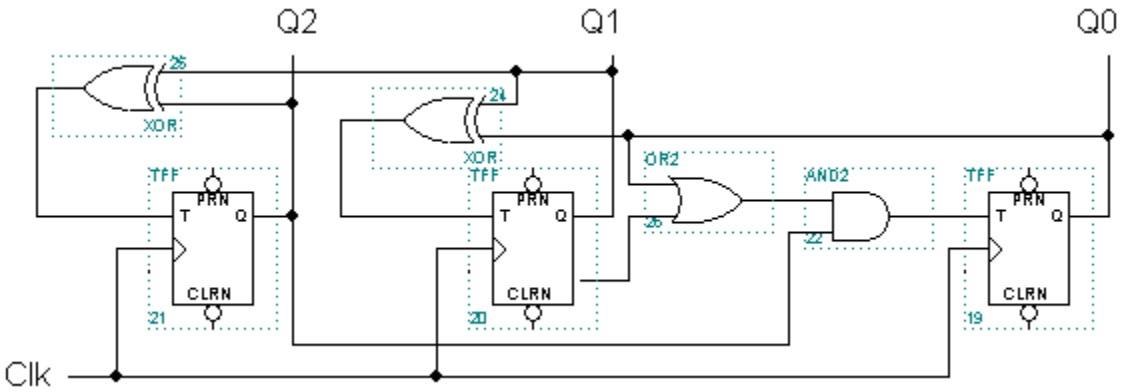
PS	NS		Output Y	
	X=0	X=1	X=0	X=1
a	b	c	0	0
b	d	e	0	0
c	f	d	0	0
d	a	a	1	0
e	a	a	0	1
f	a	a	0	0

Reduced State Table

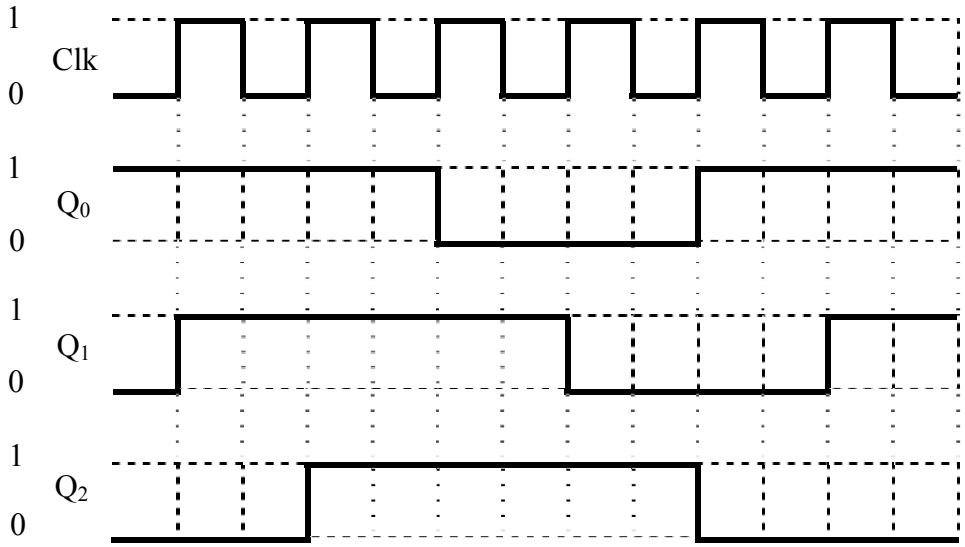
c)
d,e are adjacent
d,f are adjacent
e,f are adjacent
b,c are adjacent

d:000	b:001	c:011	f:010
e:100	a:101	----	----

Q.3) [30 pts]
Consider the following 3-bit synchronous counter circuit.



a) Complete the following timing diagram. (Note that initially $Q_2Q_1Q_0 = 001$)



b) Reimplement the above counter using JK flip-flops **ONLY**. Draw the circuit diagram.

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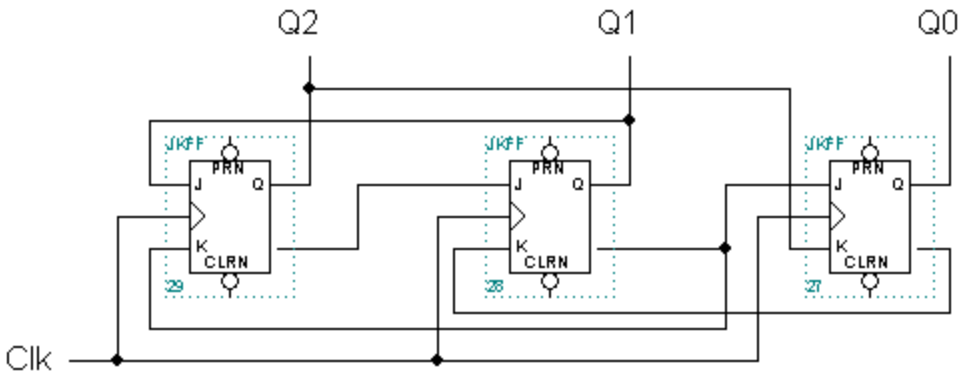
b)

Present State			Next State			Flip-Flop inputs					
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_{Q2}	K_{Q2}	J_{Q1}	K_{Q1}	J_{Q0}	K_{Q0}
0	0	1	0	1	1	0	X	1	X	X	0
0	1	1	1	1	1	1	X	X	0	X	0
1	1	1	1	1	0	X	0	X	0	X	1
1	1	0	1	0	0	X	0	X	1	0	X
1	0	0	0	0	1	X	1	0	X	1	X

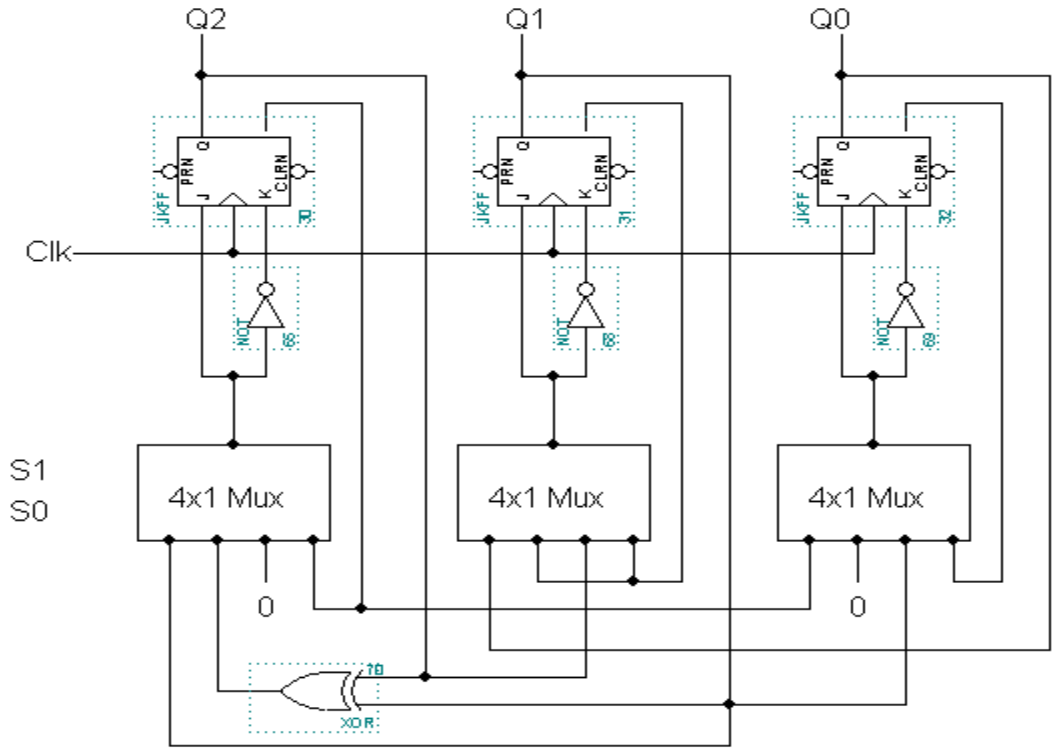
Using K-map (you have to show this):
$J_{Q2} = Q_1$ $K_{Q2} = Q_1'$ $J_{Q1} = Q_2'$ $K_{Q1} = Q_0'$ $J_{Q0} = Q_1'$ $K_{Q0} = Q_2$



Q.4) [24 pts]

Consider the following synchronous sequential circuit that operates in different modes according to the inputs S_1S_0 that are connected in parallel to all Multiplexers selections. Analyze the circuit and fill in the below table.

Note: For S_1S_0 = 10 and 11 cases, assume that initially $Q_2Q_1Q_0$ = 000



S_1	S_0	Circuit Operation
0	0	Complement the outputs
0	1	Shift right
1	0	Even up-counter (0,2,4,6,0,…)
1	1	Johnson counter (000, 001, 011, 111, 110, 100, 000, …)