## EASTERN MEDITERRANEAN UNIVERSITY COMPUTER ENGINEERING DEPARTMENT CMPE 224 COMPUTER ARCHITECTURE I HW\#1

Q.1. Show how an SR-FF can be constructed using a D FF and other logic gates.
Q.2. One way to avoid the undesired behavior of $\mathrm{SR}-\mathrm{FFs}$, when $\mathrm{S}=\mathrm{R}=1$, is to create a set-dominant SR -FF in which the condition $S=R=1$ cause the FF to be set to 1 . Design a set-dominant $\mathrm{SR}-\mathrm{FF}$ and show its circuit.
Q.3. Show how a JK-FF can be constructed using a T-FF and other logic gates.
Q.4. Design a 3-bit up/down counter using T-FFs. It should include a control input w. If $w=0$, the circuit should behave as an up-counter. If $\mathrm{w}=1$, then the circuit should behave as a down counter.
Q.5. Design a clocked sequential circuit with single input $w$ and single output $z$. the circuit generates $z=1$ when the last and the previous two bits on w form subsequences 010 or 110 ; otherwise $\mathrm{z}=0$. Overlapping input patterns are allowed.
Q.6. Design a clocked sequential circuit that produces an output $\mathrm{z}=1$ if it detect the presence of subsequences 001 or 011 in the input sequence along a single input line x .
Q.7. A clocked sequential circuit has two inputs $w 1$ and $w 2$, and an output $z$. Its function is to compare the input sequences on $w 1$ and $w 2$. If $w 1=w 2$ during any four clock cycles, the circuit produces $z=1$; otherwise $z=0$. For example,

$$
\begin{aligned}
\mathrm{w} 1: & 0110111000110 \\
\mathrm{w} 2: & 1110101000111 \\
\mathrm{z}: & 0000100001110
\end{aligned}
$$

Q.8. Design a moulo-6 counter which counts in the sequence $0,1,2,3,4,5,0,1, \ldots$. The counter counts the clock pulses its enable input $w$ is equal to 1 , otherwise it keeps the latest count until it is enabled again. Use D-FFs in your design.

## Q.9. Repeat Q. 8 using JK-FFs.

Q.10. Repeat Q. 8 using T-FFs.
Q.11. Design a 3-bit counter-like circuit controlled by an input w. If $w=1$, then the counter adds 2 to its contents, wrapping around 8 or 9 . Thus, if the present state is 8 or 9 , then the next state becomes 0 or 1 , respectively. If $\mathrm{w}=0$, then the counter subtracts 1 from its contents, acting as a normal down counter. Use RS-FFs in your design.
Q.12. Repeat Q. 11 using JK-FFs.
Q.13. Repeat Q. 11 using D-FFs.
Q.14. Repeat Q. 11 using T-FFs.

