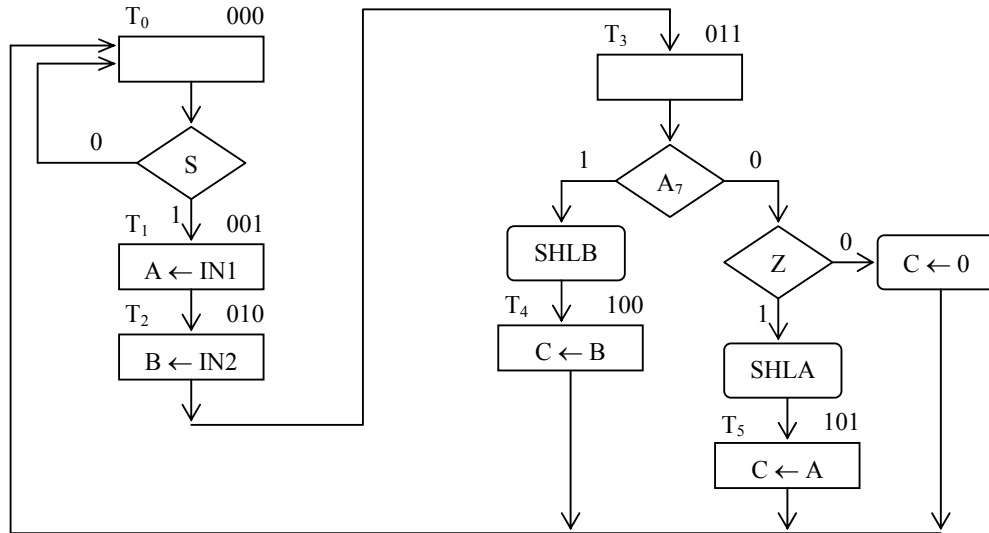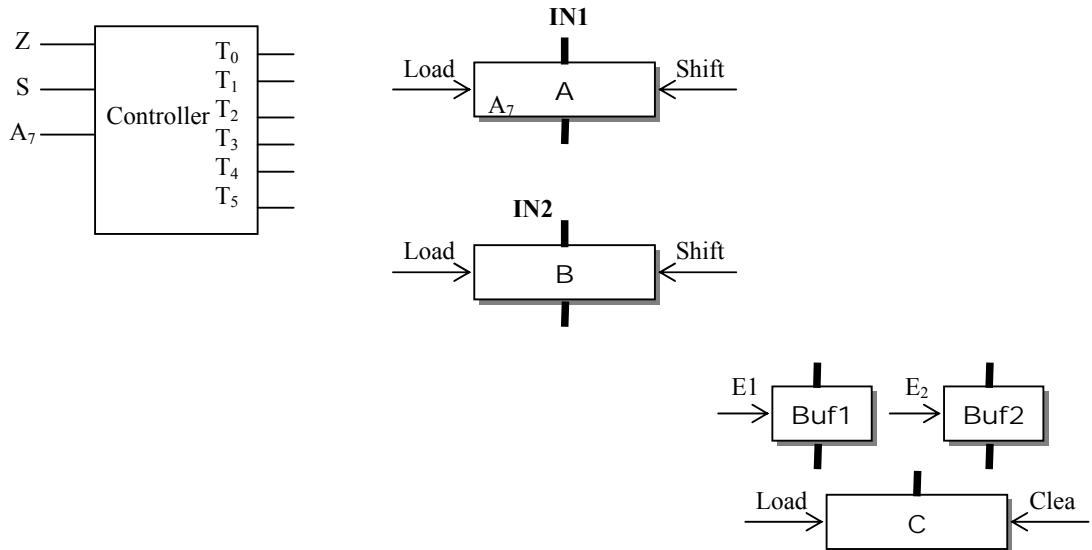# CMPE-224
Worksheet # 2

Q.1) A digital system is described by the following ASM chart. **A**, **B** and **C** are 8-bit registers with the characteristics shown below. **IN1** and **IN2** are 8-bit numbers represented in 2's complement format. The **Z** signal is equal to 0 when the contents of register A are 0's, otherwise Z is equal to 1. **Buf1** and **Buf2** are 8-bit buffers with enable inputs E_1 and E_2 respectively.

a) Complete the data-processor part of the system by showing all connections.
b) Implement the controller part of the system using MUXs.
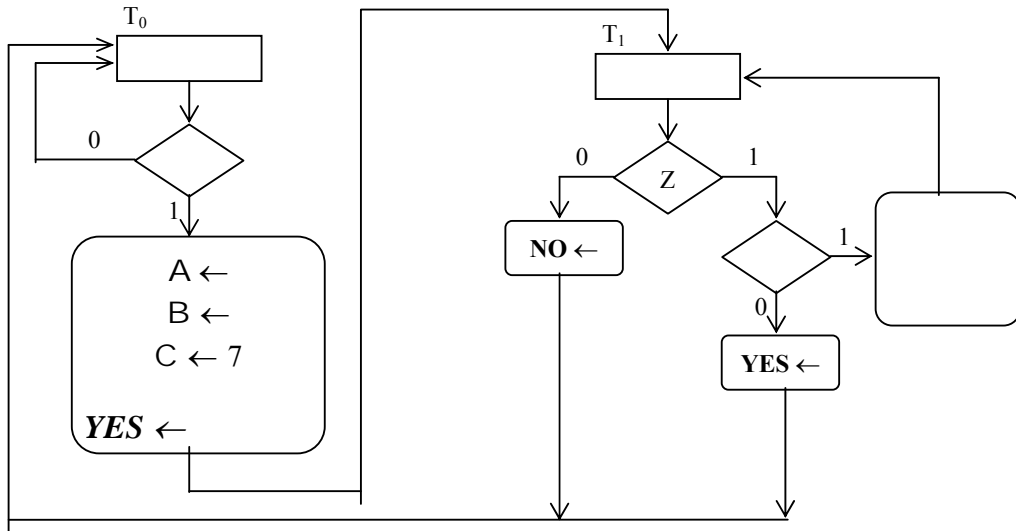**c)** Repeat (b) using minimum number of D FFs.

Q.2) A digital system is described by the following ASM chart. **A**, **B** and **C** are 8-bit registers with the characteristics shown below. **IN1** and **IN2** are 8-bit numbers that will be loaded to **A** and **B** respectively when the "**S**" signal becomes high. The system will set a "**YES**" signal if the loaded numbers are complements of each other. Otherwise a "**NO**" signal will be set, and the system returns to the initial state. These signals will be reset on receiving the next "**S**" signal. A **Z** signal (output of a 2-input XOR gate) can be used to compare the numbers bit by bit.
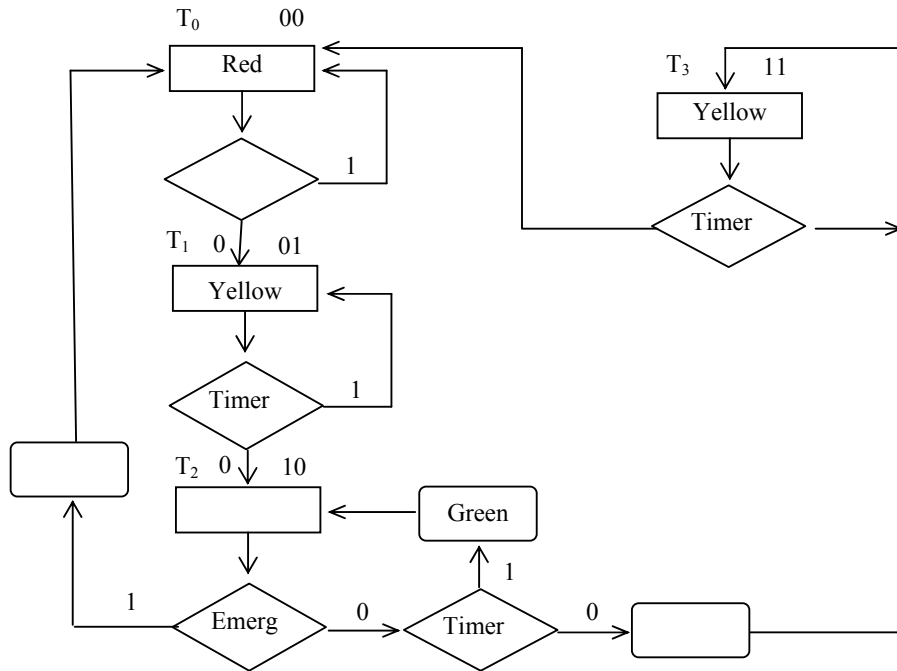

a) Complete the above ASM chart by filling the necessary items in boxes.
b) Complete the data-processor part of the system by showing all connections.
c) Implement the controller part of the system using minimum number of D FFs and gates.
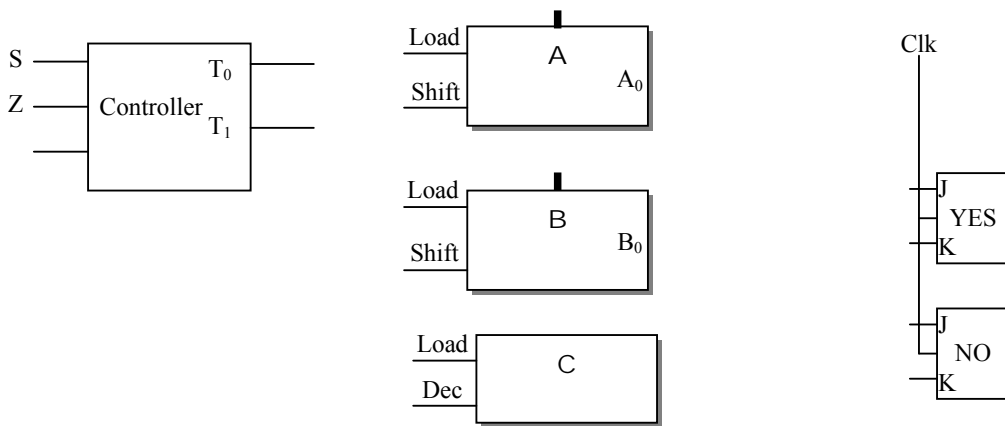
Q.3)

You are required to design a traffic light controller that can be represented by the following ASM chart. As you know there are three lights "Red, Yellow, and Green". Although not shown in the chart, assume that when the light color is changed, a timer (counter) is loaded with the appropriate period of the related signal, and then decremented every clock pulse (Assume the counter is initially automatically loaded). There is an emergency signal "Emerg" that can be used for emergency purposes to switch the light to "Red" when it is "Green".

a) Complete the above ASM chart by filling the necessary items in boxes.
b) Complete the data-processor part of the system by showing all connections except the connections for resetting the Red, Yellow and Green FFs.
c) Implement the controller part of the system using Mux'es method. Draw the circuit.

Q.4) Derive an ASM chart for the ordinary JK FF.

Q.5) Derive an ASM chart for modulo-3 counter with enable (count) input.

Q.6) You are required to design a synchronous sequential circuit which:
- Waits until an external signal S becomes high.
- When S becomes high, it loads an 8-bit register A and a 3-bit register C with non-zero unsigned external data.
- Shifts the register A to the left by a number of times equal to the contents of C. (For example if the contents of C are 111, the contents of A will be shifted 7 times in consecutive clock pulses).
- Returns to the initial state.

a) Draw the corresponding ASM chart.
b) Design the control unit using multiplexers.
c) Draw the data processor. Assume that register A has *LOAD* and *SHL* (Shift-left), and register C has *LOAD* and *DEC* (Decrement) control inputs. Write the Boolean equations for these signals.

Hint: The system can be described by two states only.

Q.7) Consider the following ASM chart:
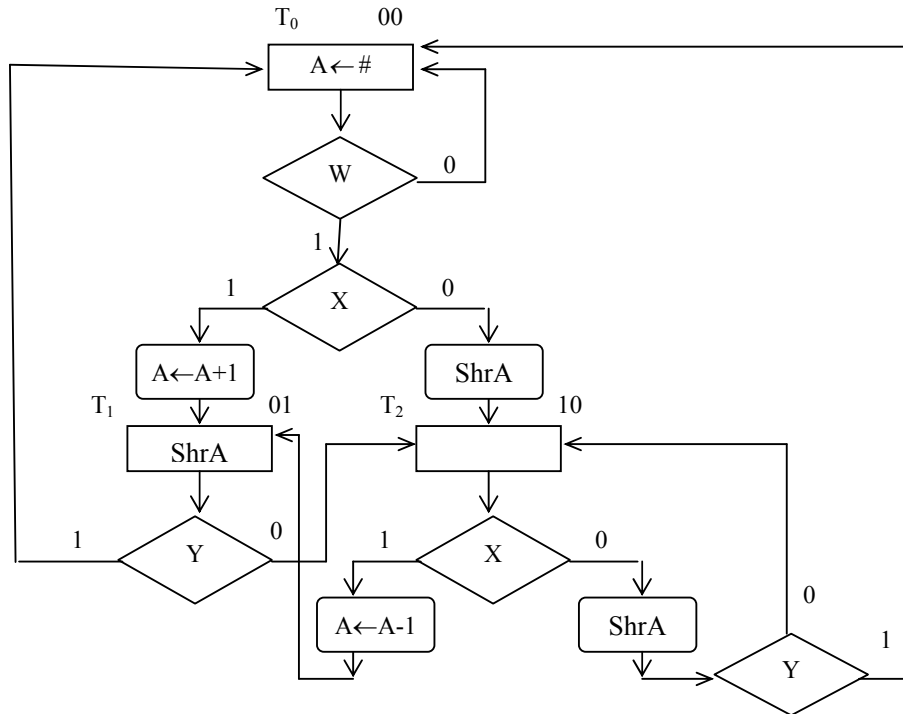
a) Assume that register A has *LOAD*, *SHR* (Shift-right), *INC* (Increment) and *DEC* (Decrement) control inputs. Write the Boolean equations for these signals.
b) Implement the controller part of the system using Mux'es method. Draw the circuit.
c) Repeat part (b) using one D FF per state.
d) Repeat part (b) using PLA method.