CMPE224 Digital Logic Systems

Department: Computer Engineering

Instructor Information
Name: Prof. Dr. Muhammed Salamah
E-mail: muhammed.salamah@emu.edu.tr
Office: CMPE 114
Office Tel: 1149

Assistant Information
Malek Al-Khatib (Room: 224); Nada Kollah (Room:101)

Meeting times and places

Group1	**Group2**
Tuesday 08:30-11:20, Room CMPE 127	Monday 12:30-14:20, Room CMPE 036
Wednesday 12:30-14:20, Room CMPE 127	Tuesday 14:30-16:20, Room CMPE 137 (Lab)
Thursday 16:30-18:20, Room CMPE 230 (Lab)	Friday 14:30-16:20, Room CMPE 036

Program Name: Computer Engineering	**Program Code:** 25	
Course Number: CMPE224	**Credits:** 4 Cr	**Year/Semester:** 2023-2024 Spring

☒ Required Course ☐ Elective Course (click on and check the appropriate box)

Prerequisite(s):
CMPE223 Digital Logic Design

Catalog Description:
This course presents the basic tools for the design of synchronous sequential circuits and covers methods and procedures suitable for a variety of digital design applications in computers, control systems, data communications, etc.. Concentration will be on widely-used design methods for synchronous sequential circuits together with their analysis and simulation in VHDL. The course continues with topics on Computer Architecture and a generic processor architecture with its Assembly language are presented in details.

Course Web Page:
http://cmpe.emu.edu.tr/courses/cmpe224

Textbook(s):
S. Brown and Z. Vranesic, "*Fundamentals of Digital Logic with VHDL Design",* McGraw-Hill, Third Edition, 2009.

Indicative Basic Reading List :
Richard S. Sandige. "***Digital Design Essentials***," Prentice-Hall 2002.
John F. Wakerly, "*Digital Design: Principles and Practices"* Pearson Education, 2006.

Topics Covered and Class Schedule:
(4 hours of lectures per week)

Week 1	A review of synchronous sequential logic(SSL), flip-flops (FFs), VHDL implementation of FFs. Analysis of clocked sequential circuits, state transition tables/diagrams. Design of clocked sequential circuits, design procedure, state reduction and assignment, flip-flop excitation tables. Design procedure & case studies.
Week 2	Design of counters.
Week 3	Registers & shift registers
Week 4	Asyncronous ripple counters
Week 5	Synchronous counters & timing sequences.
Week 6	Characteristics of ASM flow chart, timing considerations, Datapath implementation.
Week 7-8	ASM Controlpath implementation.
Weeks 9-10	
Week 11	Introduction to computer architecture
Week 12	Processor architecture
Weeks 13	A generic processor architecture MARIE

Week 14 Programming and interfacing the generic processor

Laboratory Schedule:
(2 hours of laboratory per week)

Week 4	Architectural design of synchronous sequential circuits.
Week 5	Behavioral design of synchronous sequential circuits.
Week 6	Architectural and behavioral design of registers.
Week 7	Architectural and behavioral design of counters.
Week 9	Design of synchronous digital systems using ASM charts.
Week 10	Introduction to generic RISC processor MARIE simulation environment.
Week 11	Instruction set and programming of MARIE processor.

Course Learning Outcomes:
Upon successful completion of the course, students must be able to

1. understand fundamental design procedure for synchronous sequential circuits (2 in criterion 3)
2. understand fundamental analysis procedure for synchronous and ripple sequential circuits (6 in criterion 3)
3. perform design of registers and counters: shift registers, multi-function registers, synchronous counters, asynchronous counters, and multi-function counters (2 in criterion 3)
4. make structured design of synchronous sequential circuits using VeriLog HDL (2 in criterion 3)
5. make behavioral design of synchronous sequential circuits using VeriLog HDL (2 in criterion 3)
6. understand algorithmic state machine (ASMs) charts (1 in criterion 3)
7. use ASM to perform datapath and controlpath designs (2 in criterion 3)
8. understand fundamentals of processor architecture, register sets and their functions (1 in criterion 3)
9. understand the architecture and instruction set of a generic RISC processor (1 in criterion 3)
10. simulate the behavior of the generic RISC processor through programming and interfacing (6 in criterion 3)

	Method	**No**	**Percentage**
Assessment	Midterm Exam(s)	1	25 %
	Quizzes (14/03/24 ; 16/05/24)	2	20 %
	Labs	~7	15 %
	Final Examination	1	40 %

Policy on makeup: Only one makeup exam can be given for one of the missed exams according to the University regulations.

Policy on NG grades: NG grade will be given in the following cases:
Lab attendance < 50% or
Missing both Midterm Exam and Final Exam.

Contribution of Course to Criterion 5
Credit Hours for:
Mathematics & Basic Science : 0
Engineering Sciences and Design : 4
General Education : 0

Relationship of Course to Program Outcomes
The course has been designed to contribute to the following program outcomes:
a) an ability to apply knowledge of mathematics, science, and engineering.
b) an ability to design and conduct experiments, as well as to analyze and interpret data
e) an ability to identify, formulate, and solve engineering problems.
k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

Prepared by: Prof.Dr. Muhammed Salamah	**Date Prepared:** February 26, 2024