EASTERN MEDITERRANEAN UNIVERSITY
COMPUTER ENGINEERING DEPARTMENT
CMPE 223 DIGITAL LOGIC SYSTEMS-lab 5

EXPERIMENT VI: *Basic VHDL programming of Combinational Circuits : Structural programming through NETLSTS*

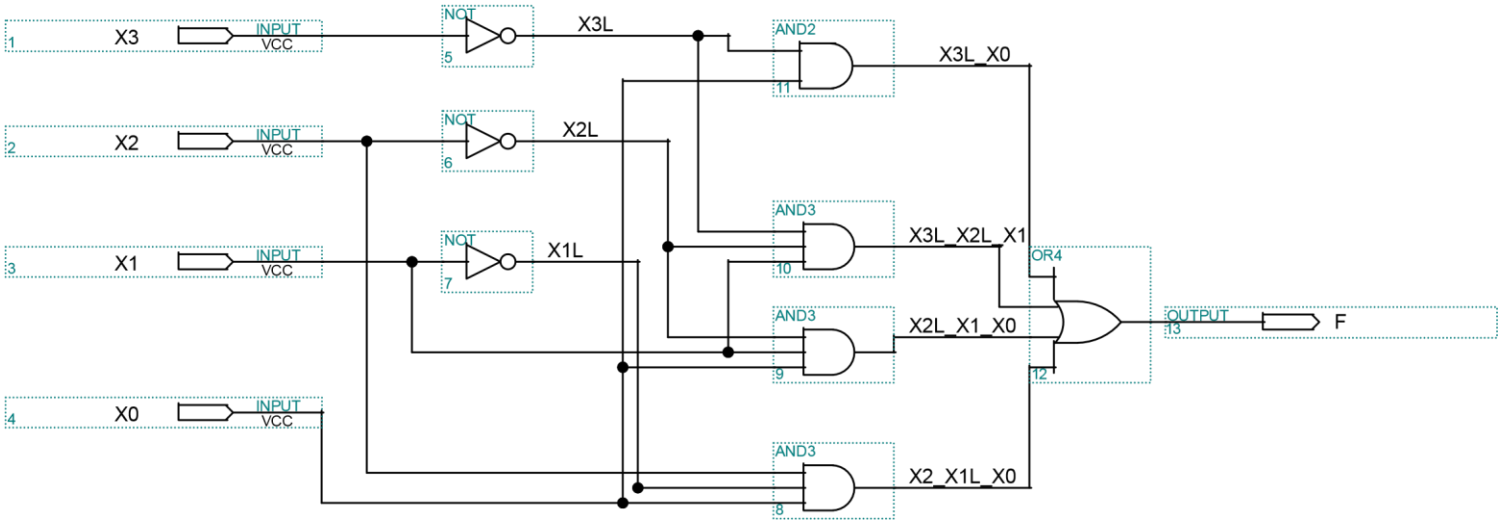
Objectives: The main objective of this experiment is to introduce the basics of structural programming of combinational circuits using VHDL hardware description language and let the students perform implementations using Quarus II system.

Preliminary Work:

Read the "Explanataions" section and Perform the Experminetal Work byusing the example given in "Explanations" section.

EXPLANATIONS: An Example of structural design with Netlists:

Consider the following circuit with input, output, and internal signal descriptions. **A signal connecting a gate output to another gate input is called a NET. The set of all nets in a circuit is called its NETLIST**. Obviously, the architecture of a combinational circuit can be described by its netlist and its output expression can be derived from the logical expressions of individual nets. Signal corresponding to a netlist are local variables associated with architecture and they are defined within the architecture block using the **SIGNAL** statement, as indicated in the following example:



The VHDL code implementing this combinational circuit using the netlist structural approach is as follows:

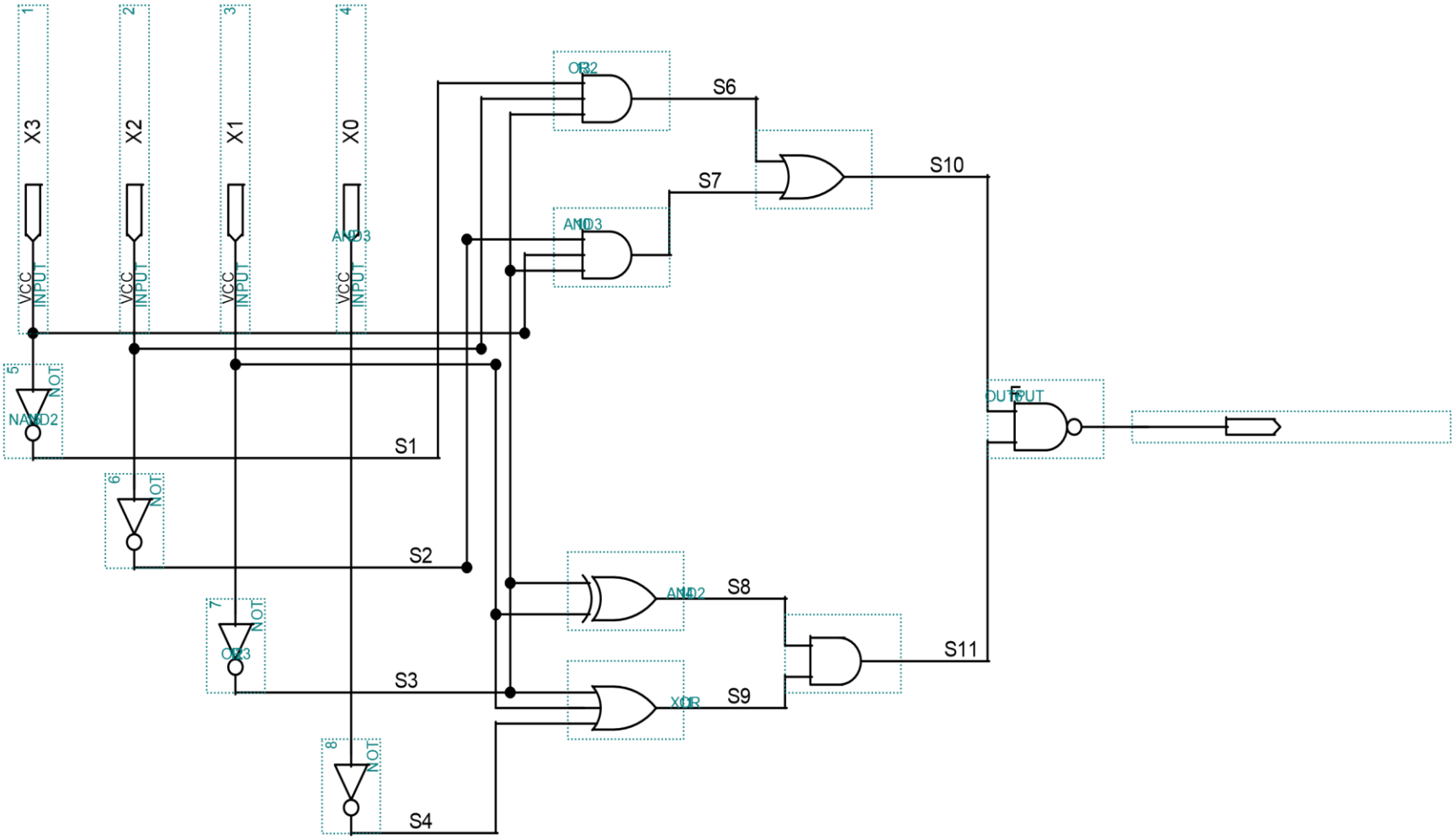
```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
ENTITY lab6 IS
PORT (x0, x1, x2,X3 : IN STD_LOGIC;
F : OUT STD_LOGIC);
END lab6;
ARCHITECTURE Arch_NelistStruct of lab6 is
SIGNAL X3L, X2L, X1L, X3L_X0, X3L_X2L_X1, X2L_X1_X0, X2_X1L_X0:STD_LOGIC;
BEGIN
X3L <= not X3;
X2L <= not X2;
X1L <= not X1;
```

```
X3L_X0 <= X3L and X0;
X3L_X2L_X1 <= X3L and X2L and X1;
X2L_X1_X0 <= X2L and X1 and X0;
X2_X1L_X0 <= X2 and X1 and X0;
F <= x3L_X0 or X3L_X2L_X1 or X2L_X1_X0 or x2_X1L_X0;
END Arch_NelistStruct;
```

Preliminary Work:

1. Given the following combinational circuit,

A. Write down the Boolean expressions for each of the netlist signals from S1 to S11.
B. Write down the Boolean expression for the output function F, in terms of the netlist signals.
C. Write down a VHDL code describing this circuit using the netlist structural approach (Look at the example).
D. Draw the Truth Table for the given circuit.
E. Compile and simulate your design using Quartus II software.
F. Compare your simulation results with the truth table of the circuit.


X3
X2
X1
X0
VCC
INPUT
NOT
NAND2
AND3
OR2
AND2
XOR
OUTPUT
F
S1
S2
S3
S4
S6
S7
S8
S9
S10
S11

NOTES:

1. You should come to the laboratory with well-prepared preliminary work.

2. Your preliminary work must be prepared by yourself, it is encouraged to exchange ideas with your friends, but the final work done must be of your own.

3. Lab duration is 2 hours and it is not possible to extend it. Hence, you should finish experimental work and prepare the experimental report in 2 hours; no delay to the next day or to the next week is possible.

Good Luck

Dr. Adnan Acan
Dr. Muhammed Salamah
Dr. Omar Ramadan