EASTERN MEDITERRANEAN UNIVERSITY
COMPUTER ENGINEERING DEPARTMENT

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CMPE 325 - Computer Architecture II

EXPERIMENT 4

Introduction to Circuit Synthesis Using ALTERA MAX-PLUS-II VHDL Tools.

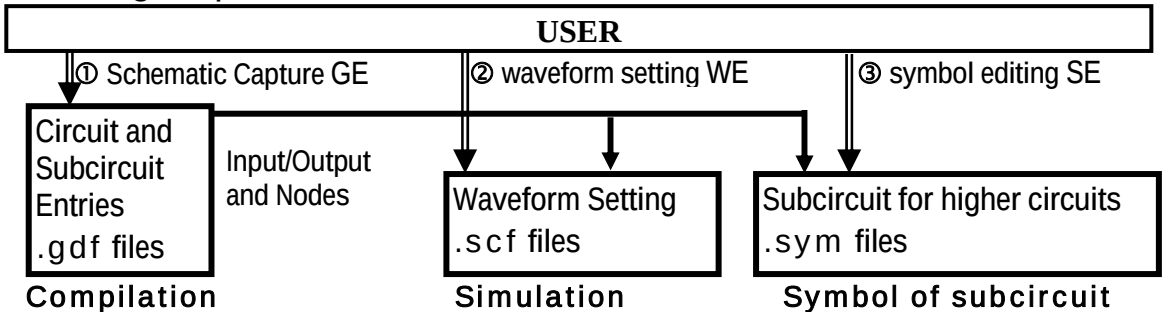
Objective: To get familiar with the VHDL development and simulation tools by generating a full adder circuit entry using the graphical capture.

1. Introduction

VHDL is an abbreviation for the VHSIC Hardware Description Language, where VHSIC is acronym for the Very High Speed Integrated Circuits. It is originated from the standardization efforts of US. Department of Defence to provide a convenient and precise form of communication for the defence contracts. Today, the digital circuits are mostly implemented with digital programmable logic devices namely SPLDs CPLDs and FPGAs.

In Altera MAX PLUS II (shortly MP2) environment, it is possible to develop all implementation phases of a circuit, or a subcircuit, including its simulation and programming into a suitable programmable IC device. The language, and the VHDL source codes occupy an important portion of the circuit implementation. However, there are tools alternative to the VHDL source coding, such as the description of the circuit behavior using its truth-table, input-output waveforms, or graphical schematic capturing. In this laboratory work you will use the schematic capture tools in MP2 to implement an 8-bit adder circuit. At the end of this experiment you are expected to be able to implement combinatory circuits in VHDL environment starting from the basic logic gates and inverters, and to simulate its circuit behavior for any input signal sequence.

The implementation process of a circuit entry is accomplished by the following steps.



2. Experimental Practice

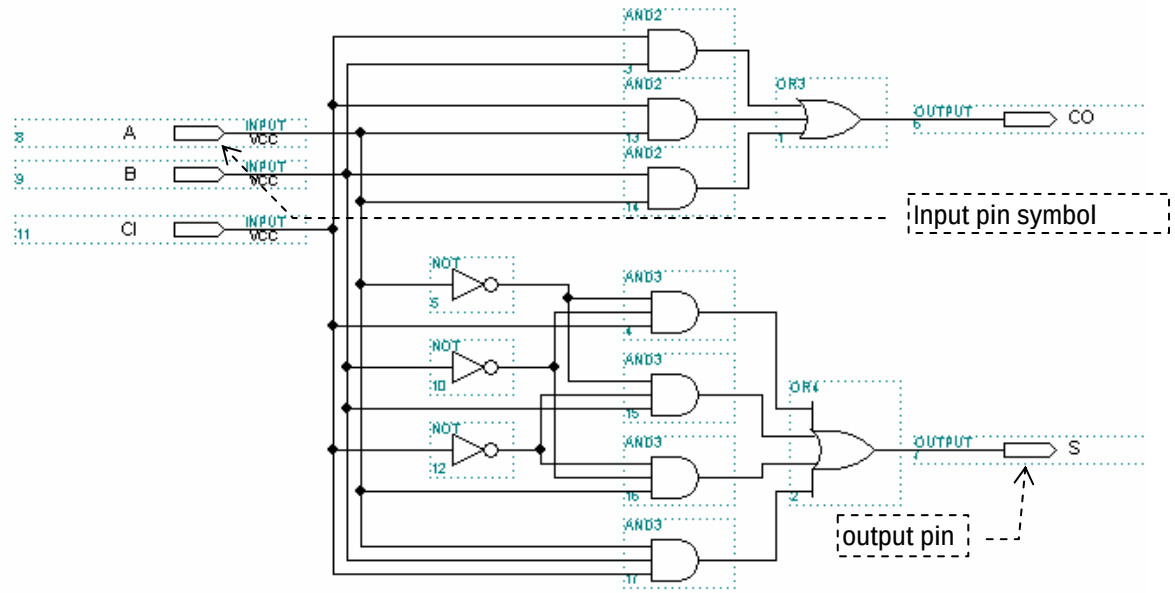
We will implement a full adder, an 8-bit adder, and compare the multiplication algorithms by simulation.

2.1 Building a single-bit full adder circuit entry

1. Start the MAX+plusII 1Ø.2 Baseline design environment.

2. Start an empty Graphics Editor Page (Alt-F,N,G,↵).
   Save it with the name onebitadd.gdf (Alt-F,S,write the name, select the folder,OK).

3. Place the following symbols into your GE page (click where to insert it, then Alt-S,E, double-click on the library, double click on the symbol.)
   a- three input pins, rename them to A, B, CI (double click on PIN_NAME, delete, and write the new-name)
   (library ..\prim symbol input)
   two output pins (rename them to S and CO)
   (library .....\maxplus2\prim symbol output) and
   three inverters (library .....\maxplus2\prim symbol not)
   b-three 2-input AND gates (library prim, symbol name and2)
   one 3-input-OR gate (library prim, symbol name or3),
   c- four 3-input AND gate (library prim, symbol name and3)
   one 4-input OR gate (library prim, symbol name or4)
4. Use the rubberbanding-tools (Junction /Connect /NoConnect) of the GE-tool-palette to connect the following full-adder circuit, that generates
   CO = A B + A CI + B CI ; and
   S = A B Ci + A' B' Ci + A B' Ci' + A' B Ci' .



5. Save the GE page frequently while you draw (Alt-F,S).

2.2 Compilation of the captured circuit entry

1. Using [*File* | *Project* | *Set Project to Current File*] or (Cntrl-Shft-J) start a project for this GE file with the same filename. Then use [*Assign* | *Device*] or (Alt-A,D) to open the Device window.

   Select *FLEX1ØK* for *Device Family*, and *Auto* for *Devices*. Click *OK* to close the device window.

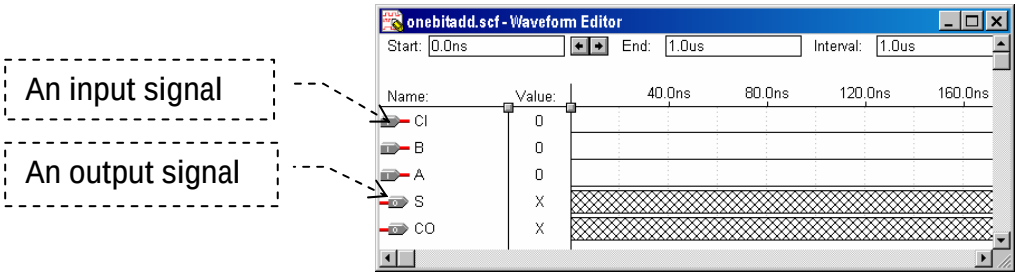
2. Use [*Max-PlusII* | *Compiler*] to open the compiler window, and start the compilation (or Alt-M,C,S). You shall get a message that "Project compilation was successfull with Ø errors, Ø warnings". Click OK in the message window. Close the compiler window using its cancel-box  at the top-right corner.

2.3 Simulation and Waveform Display

1. The hierarchy project top file of our design entry is "onebitadd.gdf" file. You can view all files connected to the projec top in the hierarchy display window [*MAX-plus-II* | *Hierarchy Display*].

   If there is no .scf file in the hierarchy display, then create a Waveform Display window **[** *File* | *New* select Waveform Editor File click OK].

   Save this window immediately using **[** *File* | *Save*] with the file name "onebitadd.scf" (this name will appear as the default-name in the file-name box).



2. Add all input and output nodes into the waveform display window [*Node* | *Enter nodes from SNF* click List, select all input and output nodes, click OK].

   Set the grid size to 1ØØ ns **[***Options* | *Grid size*].

3. Entering a grid-size-dependant clock signal:

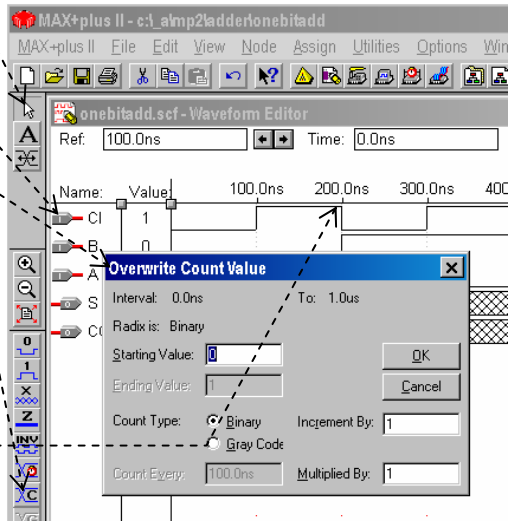
① click on selection-tool

② click on input-CI

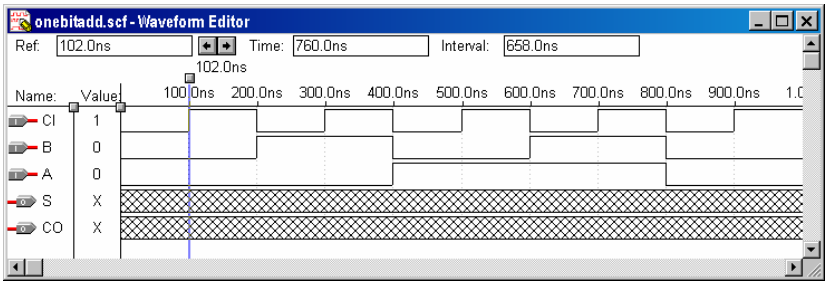
③ click on clock-tool.

④ In the Overwrite Count Value window enter count type binary
starting value = Ø
increment by = 1
multiplied by = 1
and click OK.

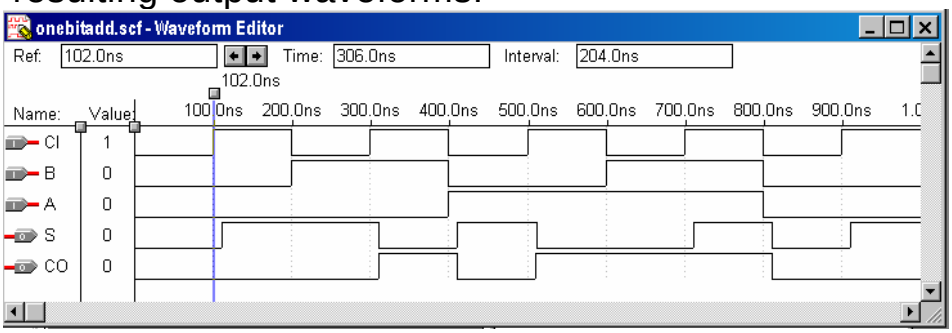
⑤ The signal CI will turn to a square wave with 2ØØ ns



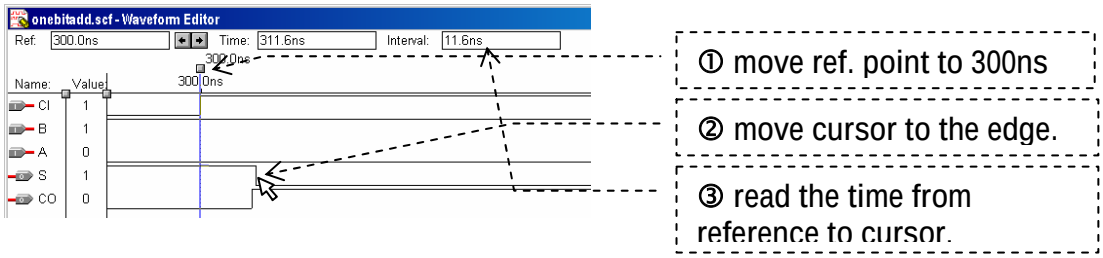
4. Without changing the grid-size, set the inputs A and B to clock dependent waveforms with "multiplied by = 2" for B, and "multiplied by = 4" for A.



5. Save the .scf file, and start the simulation by using **[** *MAX-plus II* | *simulator* | start]. There will be a message about the number of errors and warnings. If the result is Ø errors, open the .scf file to observe the resulting output waveforms.



If you set the reference line and zoom in (tool-palette ) you can measure the propagation delay in the output waveforms.



Fill in your observations to the reporting sheet.

2.4 Creating a SYMBOL for the ONEBITADD entry

6. Open a symbol editor window [*File* | *new* | *SymbolEditorFile*✓, OK]. Save the symbol with the name onebitadd (default).

Double-clicking on the left border of the blue box opens the *Enter-Pinstub* window. Write **CI** into Full Pinstub name. Select Input-pin for I/O type, and Used for Default Status. Click OK to close the *Enter-Pinstub* window. Insert the other pinstubs for A and B inputs, CO, and S outputs. Draw lines and rectangles to get a similar look to the sample symbol drawing.

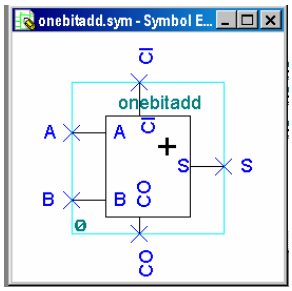


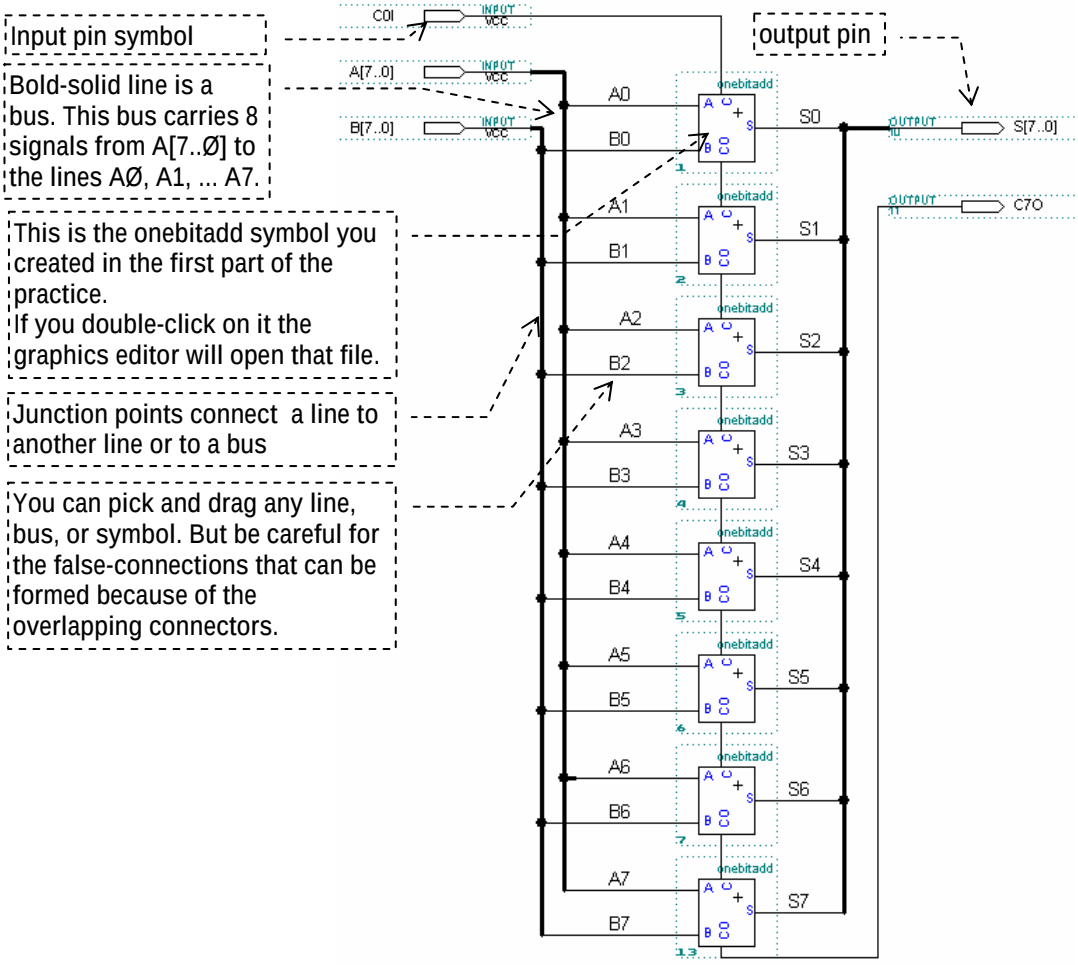
Figure 2-1 Sample symbol drawing

Save the symbol again (toolbar  or **[** *File* | *Save*]). Now your subcircuit onebitadd is ready to be inserted in another circuit for a hierarchical circuit schematics.

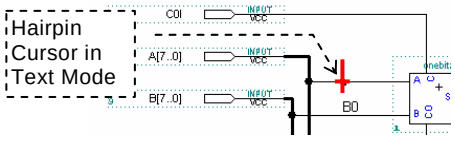
2.5 An 8-bit full adder circuit entry

1. Start an *empty Graphics Editor Page.* Save it with the name **8bitadd** into the same project folder with the onebitadd project.
2. Place the following symbols into your empty GE page
   From *prim* folder:
   Three input symbols with the names CØI, A[7..Ø], and B[7..Ø] Two output symbols with the names C7O and S[7..Ø] .
   From the *onebitadd* project folder:
   Eight copies of onebitadd.
3. Connect the symbols as shown below:

CØI is carry-zero-input
C7O is carry-7-output



The thick lines are the signal buses that are carrying many signals. Use [*Options* | *Linestyle, thick-line*] to make a line thick. The labeling is an essential part of the connection. The lines labeled AØ, A1, A2, ... A7 can be referred by a bus label A[Ø..7].



To insert these labels, use text tool in the tool palette A (or Fn2). The cursor will change to a hair-pin + with a cross. Move the cross to the connector to be labeled, and write the labels, i.e., "AØ", "A1" etc. After labeling, restore to default tool

(selection tool) by pressing esc-key. Save your circuit schematic frequently and after the circuit is completed.

2.6 Compiling 8bitadd entry

The circuit is ready in the graphics editor window, and has been already saved to the file. Before starting the compiler you have to set up a project for **8bitadd** entry.

MP2 project setting can be updated for the currently open active file in use [*File* | *Project* | *Set-project-to-current-file* (or cntrl-shft,J)]. You can check the current project using the Hierarcy Display (Alt-M,H), and return to Graphic Editor (shorcut keys Alt-M,G). After setting the project, assign the device to Flex1ØK family (Alt-A,D and select device Flex1ØK), and start the compilation of the circuit (Alt-M,C and start). If you get no error and no warnings, compile will end successfully.

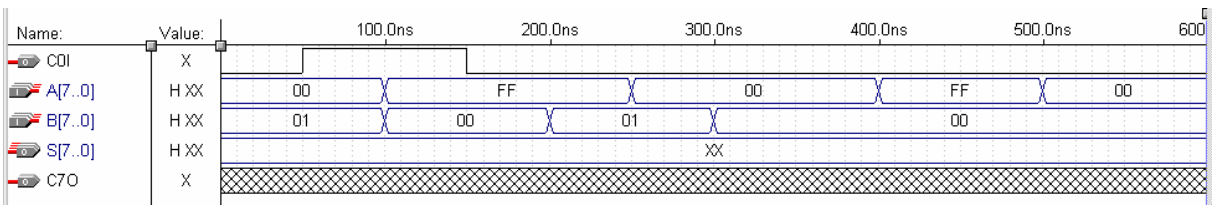
2.7 Simulation of the 8 bit addition

For the simulation of the 8-bit addition, you need a waveform set for this circuit. While 8bitadd is your project file, open a new waveform file, and save it with the name 8bitadd. Then add all input output nodes in the compiled project (Alt-N,E, list, select CØI, C7O, A[7..Ø], B[7..Ø] and S[7..Ø] , then click OK).

1- Set the grid-size to 1Øns (shortcut Alt-O, G, enter 1Øns, OK).

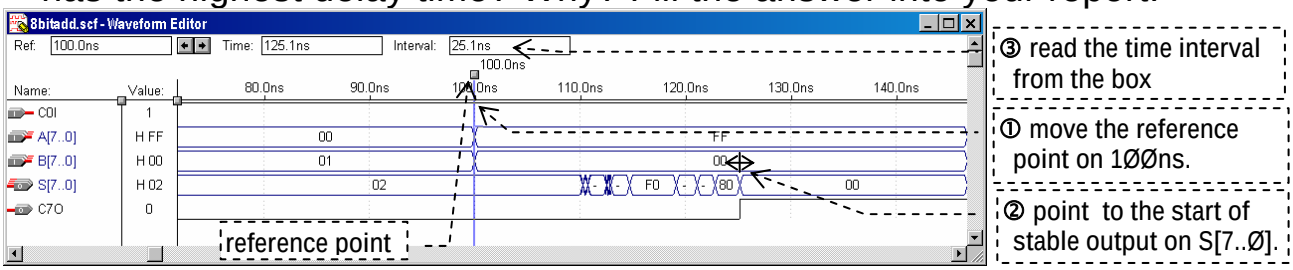
2- Set the End-time to 6ØØns (shorcut Alt-F,T, enter 6ØØns,OK).

3- Use wave-divide tool  (shortcut Fn3) to divide CØI from 5Øns to 15Ø ns. Division will take the value 1 since it started in the Ø region. Use the divide tool for A[7..Ø] to assign ØxFF to the region from 1ØØ to 25Øns, and from 4ØØ to 5ØØns (again 0xFF). Divide B[7..Ø] and assign ØxØ1starting from Ø to 1ØØns, and from 2ØØ to 3ØØns. Your waveform shall look like this:



4- Save the Waveform (Alt-F,S), and start simulation (Alt-M,S,S).

5- After simulation terminates successful, open the waveform editor and measure the output stabilization time of the 8bitadd circuit for the cases starting from 1ØØ, 2ØØ, 3ØØ, 4ØØ, and 5ØØns. Which of them has the highest delay time? Why? Fill the answer into your report.



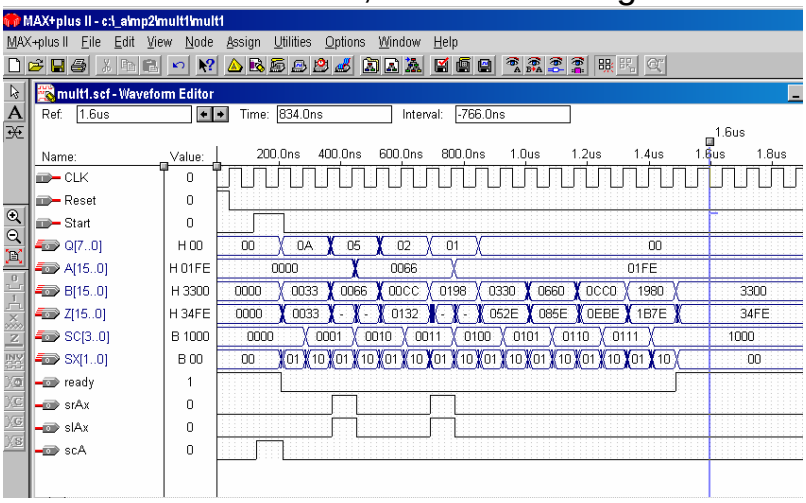
2.8 Simulation of 8-bit Multiplication Circuits

In this part of the Experiment you will simulate the 8-bit First- and Second-Multiplication circuits. These circuit entries provide a large set of component examples and a technique for implementing Mealy type ASM or FSM charts.

1- Create a new working folder for you project, and copy the files from the mult1.zip into your new working folder. Then open the graphics file mult1 in MP2. Your graphics editor will open the first-multiplication circuit. Explore how the circuit has been built, and which signals are sent from the controller. You can trace the lines inside the blocks by clicking on the symbols.

2- The folder also contains a waveform file for your simulation. Set the project active while the mult.gdf window is open and active. Compile the project. Then start the simulation, and open the waveform file. Click to zoom all tool in tool-palette. You will see the complete simulation of Øx33 by ØxØA in the waveform display.

3- Looking at the stabilization time of the ALU, find out the highest possible clock frequency for the circuit. Calculate how long it takes to find out the product (ready line low period) at the present clockrate and at the maximum possible clockrate. Fill in your answers to the report sheet.



4- Start a new project folder "mult2" and apply the same procedure for the circuit MULT2.GDF. Fill your answers into the reporting sheet.

3. ALTERA MAX+plusII 10.2 Baseline Commonly Used Procedures

This section is a procedural manual prepared for the minimal needs of the Computer Architecture students to use MAX+plusII (MP2) VHDL graphical user applications in the shortest time. It is assumed that the student have an already installed MP2 software on the computer. For the installation procedures please refer to the related section.

3.1 Introduction and Starting MAX+plusII 10.2 Baseline

MP2 VHDL development environment is a combination of 11 software packages related to the hardware description, debugging, simulation, and programming into a suitable Field Programmable Gate Array device. The programs are managed by a manager program that is called MP2 in this manual.

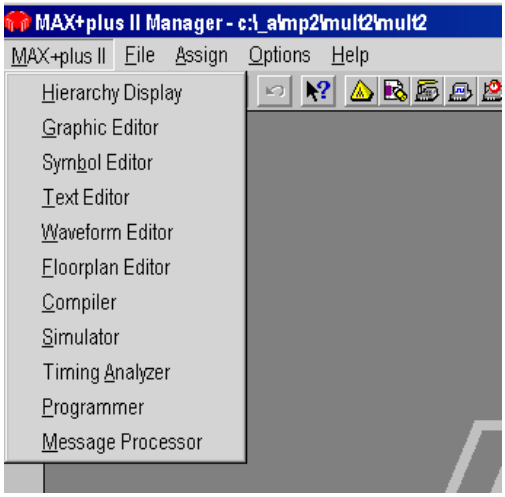
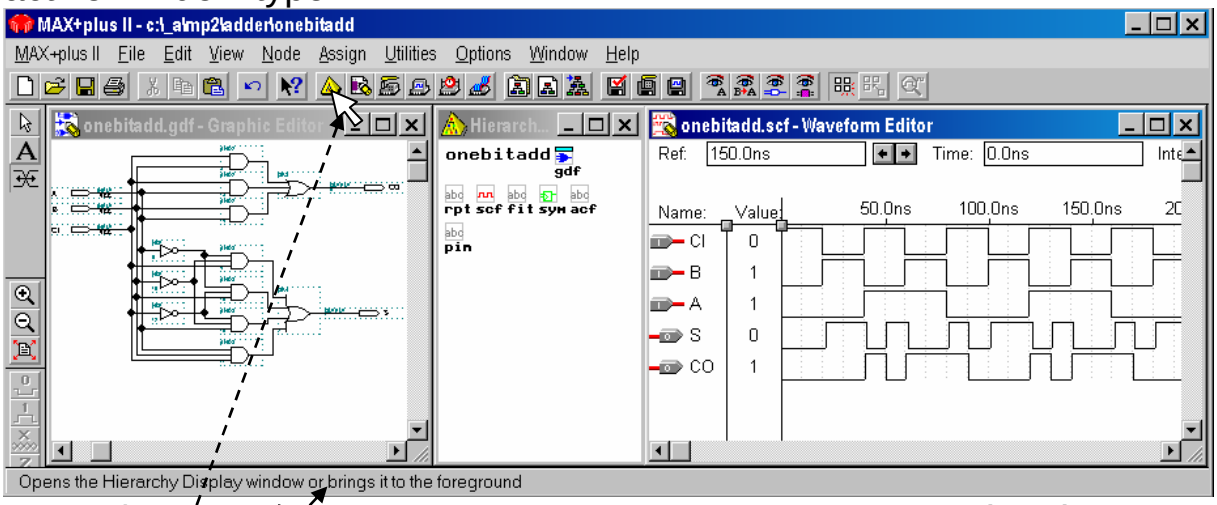


Figure 3-1 MP2 Program Modules

The Manager program starts with a left-click of mouse on the MAX+plusII 10.2 Baseline item in the START | All Programs | *MAX+plusII 10.2 Baseline* menu of the Windows XP Toolbar. The other packages in MP2 are started using MAX+plusII dropdown menu in the upper toolbar of the Manager (Main) window. In MP2, the main-menu, tool-box, and the tool-palette changes with the active window type.



While the cursor points an active commanding item an explanation appears at the bottom of the MP2 window.
Additionally, MP2 has a very detailed help menu **[*help*]**.

3.2 Procedure to Start the MP2 Manager program

Open *MAX+plusII 10.2 Baseline* (WindowsXP *START* | *All Programs* | *MAX+plusII 10.2 Baseline* | *MAX+plusII 10.2 Baseline*). After an opening ceramony the program will open to a grey window at the mid writing **ALTERA MAX+plus II** in large characters. The *main-menu* is always visible. You can **turn the *main-toolbox* on or off** using the [*options* | *preferences*] from the *manager menu*.

The programs Hierarchy Display, Graphic Editor, Symbol Editor, Text Editor, Waveform Editor, Floorplan Editor, Compiler, Simulator, Timing Analyzer, Programmer, and Message Processor can be started using the MAX+plusII dropdown menu.

3.3 Graphic Editor (GE) Procedures:

3.3.1 Starting an empty Graphics Editor Page (GE-page)

Click Max+plusII on manager-menu-bar. From the drop-down menu click Graphic Editor. An empty Graphics Editor page shall be opened. The GE-tool-palette appears at the left-side of the main window. The default mode of the GE-tool-palette is the selection-tool  .

3.3.2 Placing a symbol to the graphics editor (GE) page

1- Click to a point in the GE page (any point of the white space) where you want to place the new symbol.
2- Click *Symbol* (or use the keys ALT+S) on menu bar. In the *drop-down menu* click *Enter Symbol* (ALT+E) .
3- Use the library *....\max2lib\plus* by double click on the library name in the library list (or use ALT-S, arrow-keys, and enter to select).
4- Use the symbol file *input* (or use ALT-F, arrow-keys, and enter to select).

The symbol shall take its place at the pointed position on the graphics editor page.

3.3.3 Copying a symbol in the graphics editor (GE) page

From the *GE-tool-palette* click the selection tool **(** **)** by your mouse (or press F1-key). Then select the symbol with a left mouse click when the mouse-cursor is on that symbol. The selected symbol appears in bold-red box. Use **[** *Edit* | *Copy* **]** from main-menu (or CTRL+C keys) to copy the symbol to the clipboard. Click to a point in the graphics editor page where you want to place the item from the clipboard. Then use **[** *Edit* | *Paste*] from main-menu (or CTRL+V keys) to paste a copy of the symbol to the page.

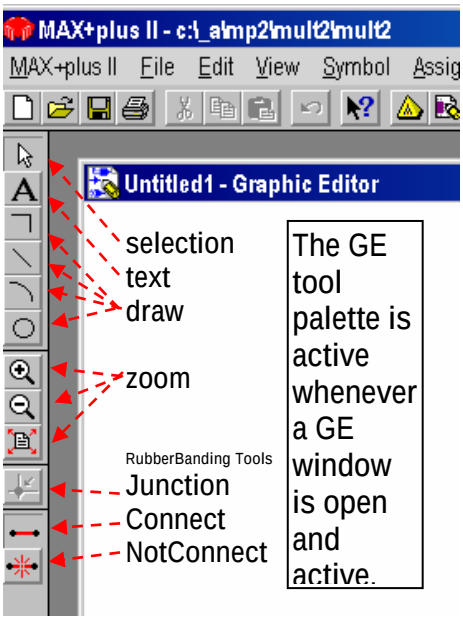


Figure 3-2 GE tool palette contents

3.3.4 Moving a symbol in the graphics editor page

From the *GE-tool-palette* click the selection tool (*, or esc-key*). Then with your mouse move the cursor-arrow to the symbol you want to move. While the arrow is pointing the symbol push and keep the left button of the mouse pushed. You can **drag** the symbol with the mouse until you release the button. Drag the symbol to the desired place in the page.

If the connect tool is active while dragging a symbol, the connection lines of the symbol will get dragged together with the symbol. To prevent dragging of the connecting lines the connect tool is deactivated by clicking on the Not-connect tool .

3.3.5 Changing the name of an input or output pin

With the *select-tool* of the GE-tool-palette double click on the **PIN_NAME** to select the text to be changed.
The selected text appears in a bold-red box.
Use the arrow-keys to move the text-cursor in the text.
Use the shift+arrow-keys to block-select a portion of the text.
Use backspace-key (←) to delete the text.
Use character keys (A..Z,a...z,0..9,_) to write the new name.

3.3.6 Connecting the symbols

If both the selection-tool and the connect-tool are turned on, on a pinstub of a symbol the cursor will change to the drawing hairpin (+). Consequently, click and drag will start a connector line. The terminal points of the lines are also active points to continue to draw the

connector. A solid-bold line extends in solid-bold form, and a solid-normal line remains solid-normal when it is extended.

A solid line in the graphics windows is a connector, and thus the connectors can also be drawn using the line-draw-tool of the tool-palette. Similarly any bold-solid line is a multiple-connection, and can be drawn by changing the line-attribute.

3.3.7 Text, and Labeling the Connectors

In GE, the connections between the pinstubs, lines and buses can also be obtained using the same connector labels instead of connecting them by solid lines. The labeling convention of the conductors is:

1- Labels are case insensitive and a label must start with an alfabetic character: "A", "loadA", "Count" are typical valid labels.
2- Labels ending with a number are collected to a bus and can be represented by the index-list: i.e., A2, A3, A4, A5 can be carried on a single bus (solid-bold-line) that is represented by A[5..2].
3- A connection line gets the name of the connected input or output pin: i.e., a connector named A[7..0] can not be connected to the line labeled B[7..0], but A[0..7] can be connected to A0, A1, ... , A7.

3.4 Symbol Editor (SE)

3.4.1 Opening a New Symbol Editor Page

From the [*max-plus II* | *symbol editor* **]** opens a new symbol editor window. The symbol to edit appears as a blue rectangle that has a name in it.

3.4.2 Changing the Symbol Name

Click on the name, then
use **arrow keys** to move the text cursor,
backspace to delete the characters, and
alphanumeric keys to write a name.

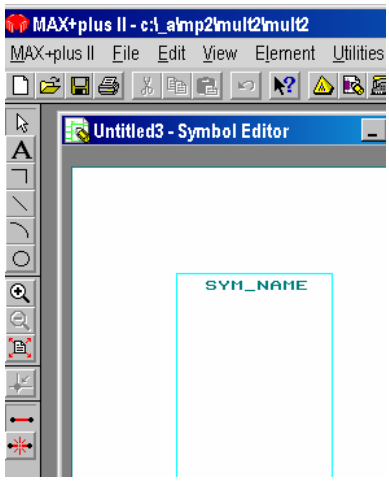


Figure 3-3 SE and GE tool-palette are almost the same in function.

3.4.3 Placing an *input pinstub* to the Symbol.

Move the mouse-cursor onto the left border of the blue rectangle.
On the blue rectangle double-click to open the *Enter-Pinstub* window.

Write the corresponding name into *Full Pinstub* ***name*** **box**.
Select *Input-pin* for I/O Type, and *Used* for Default Status.
Click *OK* to close the Enter-Pinstub window.

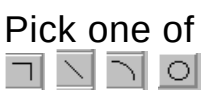
3.4.4 Dragging a pinstub of a symbol

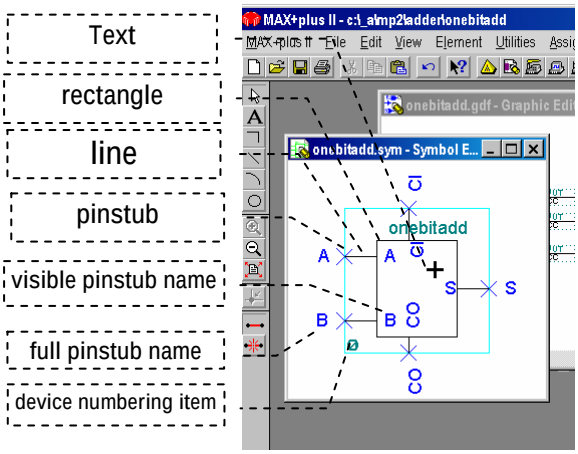
Move the mouse-cursor on the **pinstub-cross mark**. Press the left mouse-button and keep it pressed (= grab the cross-mark) while moving the pinstub along the symbol border.
Release the button when you have it at the desired location.

3.4.5 Resizing the symbol rectangle

To shrink the symbol, grab the device-numbering item at the left-bottom corner of the symbol and drag it to a suitable location since otherwise it might block moving the borders. Then grab the border and drag to the desired size.

3.4.6 Drawing rectangles, pin-terminals, and Text

Pick one of the drawing tools  to place a text or a shape in your symbol. Click and keep pushed on the symbol at the point where the shape must start. While pushing the left button of the mouse move the mouse to the desired terminal point .



3.4.7 Saving the symbol to a library

Open the Save as dialog by using [file | save as] . Save the file into the project folder (otherwise symbol may not work).

3.4.8 Closing the symbol window.

Use the cross on the top-right corner of the Symbol Editor page.

3.5 Waveform editor (WE)

WE is used to select the outputs, and to generate a waveform for each of the inputs of a simulation.

3.5.1 Starting a new WE window

A waveform file of a project appears in the HD window as a .SCF file, and the Hierarchy top level shall have an SCF file to start the simulation. Use [*Max-Plus-2* | *Waveform-Editor*] to open a new WE window.

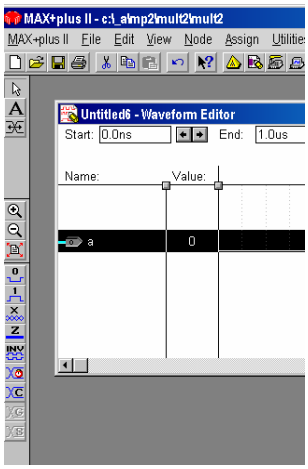
3.5.2 Renaming and Saving WE window

Use [File | SaveAs] to save WE window with different name and folder.

3.5.3 Adding a signal into WE

Double-click in the Name column and select Enter nodes from SNF from the pop-up-menu. Or, follow the main menu [Node | Enter nodes from SNF].

WE has a tool-palette with the following items to edit the waveforms.



- Pulse insert/edit tool
- Make it constantly zero
- Make it constantly one
- Make it constantly don't care
- Make it constantly high empedance
- Complement the selected waveform
- Create square waveform
- Create a counter-based waveform

3.5.4 Setting the grid size

The synchronous signal are created synchronous to the grid-size. The grid size is set using [Options | Grid size].

3.5.5 Square Waveforms synchronous to the Grid

Use [*Edit* | *Over write* | *Count value*] (or) to form a square-wave with the period multiples of the grid-size.

3.5.6 Any waveform by dividing the time

Use pulse insert edit tool to divide a partition of the waveform and to assign the desired value to the waveform.

3.6 Other Programs started from the MP2 Manager

3.6.1 Hierarchy Display (HD)

HD displays

① The starting source-file of the project, which is called the Hierarchy Top File. It can be a Text-source (VHDL file ⇒.VHD) or a graphics-source (graphics design file ⇒.GDF)

② All files linked to the Hierarchy Top File.

You can use the HD window to check the existence of the necessary files that should exist in the project for the programming or simulation steps. You can click to open a file that appears in HD for editing if you want to change some of the parameters or entries in that file.

3.6.2 Text editor (TE)

TE is a convenient text editor that indicates the VHDL keywords and comments in colored characters. It has no tool-palette, however, similar to the GE and SE programs, it modifies and extends the manager toolbar items.

3.6.3 Floorplan Editor (FPE)

FPE shows the allocation of the gate arrays for the compiled project.

3.6.4 Compiler (MP2C)

MP2C is the program that compiles the Text, or the Graphics source into the programming code of a programmable chip.

4. Installation and Getting a License Key

Altera Max plus2 (MP2) reqires licensing. To get a license for the non commercial usage of MP2

① Install MP2 (it installs to run in restricted mode). Run MP2 and click to the menu [options | license setting] , select system info

② Write the c: drive serial number (a code like this: 5ca3245c)

③ Goto MP2 pages on the web

https://www.altera.com/support/software/download/altera_design/mp2_student/dnl-student.jsp

Select from the left column Licencing

http://www.altera.com/support/licensing/lic-index.html

page will be opened. At the bottom of the page click on

MAX+PLUS II software for students & universities

Applies to MAX+PLUS II Student Edition software or

MAX+PLUS II software for University Program members

In the new page select

MAX+PLUS II Student Edition software Note (1)

[x] Version 10.2, 10.1 or 9.23

and click continue. In the opened page write the c: drive serial number into the box (the code similar to 5ca3245c) and click continue. In the next page, fill in the required boxes of the form without any empty item. It will ask also your e-mail address to send you the licence key.

④ Get the altera e-mail from the e-mail address you have written to the form. Copy the attached file licence.dat into the C:\maxplus2 folder.

⑤ In the MP2, click on [options | license | setting] to open the licence window. Select browse, and give the path of the license.dat file. Click ok, to close the license window.

⑥ Program is ready to use.

Name: _____ Student Number:_____
Submitted to (Asst.): _____ Date:dd/mm/yy ___/___/___

EASTERN MEDITERRANEAN UNIVERSITY
COMPUTER ENGINEERING DEPARTMENT

Fall 2007-08

CMPE 325 - Computer Architecture II
EXPERIMENT 4- Reporting Sheet

Section 2.3 step 4:

Write the inputs and the output delay for carry out and sum at the following time instants:

time (ns)	A, B, CI	delay for CO	delay for S
1ØØ			
2ØØ			
3ØØ			

Section 2.7 step 5:

RowNr	time (ns)	Inputs CØI,A,B	Output C7O, S	ALU-stabilization (ns)
1	1ØØ			
2	2ØØ			
3	3ØØ			
4	4ØØ			
5	5ØØ			

Which of them has the highest stabilization time? . . . . . .

Why: _____

Section 2.8 step 3 (Set the grid-size to 4Øns**):**

1a- Maximum stabilization delay at the adder output is . . . . . ns period starting at time . . . . . ns.

b- This stabilization period means clock frequency cannot be greater than . . . . . MHz.

2a- The multiplication takes . . . . . . cycles, and . . . . . ns.

b- The multiplication will take minimum . . . . . . ns if the maximum clock frequency is used.

Grading: Lab Performance:
Asst. Observations: