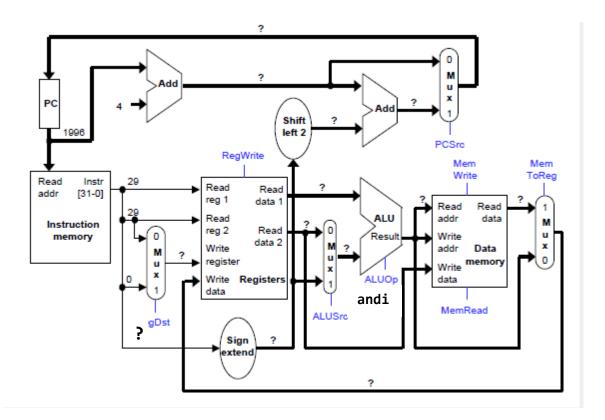
Number:	Name	:	

**CMPE324 Quiz, 2017-2018 – Spring Date:** 15/05/2017 - **Duration: 40** min.

**Q1) [30pts]** Assume that it is required to execute the following I-type immediate **and** (**andi**) instruction in the single-cycle data-path processor:

## andi \$29, \$29, 0

a) **[15pts]** The single-cycle data-path shown below shows the execution of this instruction. Several of the data-path values are filled, and you are requested to provide values for the other remaining signals in the diagram, which are marked with a ? symbol. Write your answers (in decimal) directly on the diagram. Assume register \$29 initially contains the number 129, and if a value cannot be determined, mark it as 'X.'



b) **[15pts]** Fill in the table below the correct control signals for executing **andi** instruction. Use 'X' to indicate any don't-care conditions (if necessary).

RegDst	RegWrite	ALUSrc	ALU0p	MemWrite	MemRead	MemToReg	PCSrc

**Q2)** [30pts] In a Single-Cycle Processor implementation, assume that memories and the ALU have 2ns delays, and the registers have a 1ns delay. What would be the exact CPU time of the following code segment that clears a string of length **5**bytes? \$a1will loaded with 5.

Loop:sb \$zero, 0(\$a0) # store byte in memory

add \$a0, \$a0, 1

sub \$a1, \$a1, 1

bne \$a1, \$zero, Loop

End : jr \$ra

- (a) [10pts] Cycle time = .....
- (b) [10pts] # of clock cycles .....
- (c) [10pts] Total CPU time .....
- Q3) [40pts] Consider the following Single-Cycle Processor data-path. A/ [20pts] High-light the data-path for executing the instruction

bne rs, rt, immediate

**B/** [20pts] Draw implementation of the logical function of PCSrc for this instruction.

