EMU-COMPUTER ENGINEERING DEPARTMENT
CMPE224 DIGITAL LOGIC SYSTEMS
EXERCISE QUESTIONS II

Q.1. Design a 6-bit shift register, with parallel load capability, that shifts left in two steps as follows: Q2←Q0, Q3←Q1, Q4←Q2, Q5←Q3, Q6←Q4, Q0←Q5, Q1←Q6.

Q.2. Design 4-bit a register that is controlled by two cotrol inputs S1 and S0, and operates in four different modes as follows:

S1	S0	Operation Mode
0	0	Parallel Load
0	1	Shift Left
1	0	Shift Right
1	1	Complement

Also, add an enable control to this multi-function register such that when enable input E=1, the register works as described above, but when enable E=0, the register keeps its current contents only.

Q.3.Design a 6-bit multi-function register that is controlled by two control inputs S2, S1 and S0, and operates in five different modes as follows:

S2	S1	S0	Operation Mode
0	0	0	Shift right in two steps
0	1	0	Shift left in two steps
1	0	0	XOR contents with 101010
1	1	0	XNOR contents with 010101
X	X	1	AND contents with 101010

Use D-FFs, 4x1 and 2x1 MUXs only.

Q.4. Design a 6-bit ring counter such that the counter is initialized with contents 100001. Hence, two 1's will rotate through the counter bits.

Q.5. Design a 4-bit shift register such that its contents change as 1111->0111->0011->0001->0000->1111->...

Q.6. i. Design a 3-bit ripple counter that follows the count sequence 1-0-3-2-5-4-7-6-1-...

ii. Design a 3-bit synchronous counter that follows the same count sequence using T-FFs.

Q.7. i. Design a 3-bit ripple counter that follows the count sequence 0-3-6-1-4-7-2-5-0-...

ii. Design a 3-bit synchronous counter that follows the same count sequence using T-ffs.

Q.8. Design a 4-bit mult-function syncronous counter that is controlled by two control inputs as follows:

X	Y	Operation Mode
0	0	Clear the counter (set all count bits to 0)
0	1	Count up
1	0	Count down
1	1	Set the counter (set all count bits to 1)

Carry out this design using JK-FFs.

Q.9. Design a 4-bit multi-function register/counter that is controlled by control inputs X and Y as follows:

X	Y	Operation Mode
0	0	Shift left
0	1	Count down
1	0	Count up
1	1	Shift right

Carry out this design using JK-FFs.

Q.10. i. Design a ripple counter that follows the count sequence 7-6-4-5-7-...

ii. Redesign this counter as a synchronous one using T-FFs and minimum number of external gates.

In case of any questions, do not hesitate to ask!

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