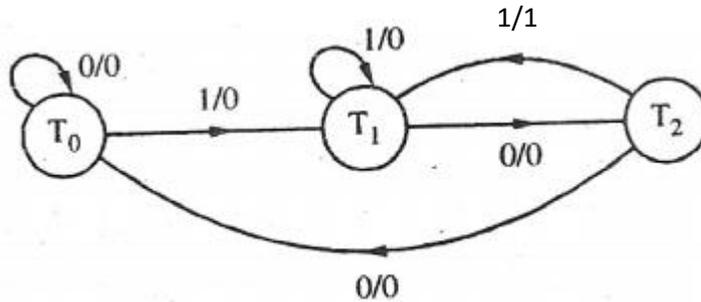


EMU-COMPUTER ENGINEERING DEPARTMENT
 CMPE224 DIGITAL LOGIC SYSTEMS
 EXERCISE QUESTIONS III

Q.1. Draw an ASM chart and state transition table to describe a sequence detector that detects a sequence of 101. Design the control unit using JK flip-flops.



Q.2. Draw the ASM chart of a synchronous digital system, with two inputs x_1, x_2 and one output z , that recognizes the input sequence of pairs $x_1x_2 = 01, 01, 11, 00$. The output z is to be 1 when $x_1x_2 = 00$ if and only if the three preceding pairs of inputs are $x_1x_2 = 01, 01, 11$ in that order. Design this systems using MUX+DFF+DEC. Use JKFFs for the datapath.

Q.3. Design a synchronous digital system that will divide two n -bit unsigned numbers using the repeated subtraction method as follows. Initially A (divident) and B (divisor) are loaded with n -bit values INA and INB , respectively. Then, the system first checks if $B=0$, and if so, the system sets the output $DIVERROR$ to 1, $DIVERROR$ is 0 otherwise. Then, the system compares the magnitudes of A and B and if $A \geq B$, the system subtracts B from A and increments a counter Q to compute the quotient of the division. Design the datapath. Then, design the controlpath using MUX+DFF+DEC.

Q.4. **Shift and Add Multiplier:** Consider the problem of multiplying two n -bit numbers A and B . This operation can be implemented using an approach similar to manual multiplication algorithm: For each bit i in the multiplier that is 1, we add to the product the value of the multiplicand shifted to the left i times. This algorithm can be described in pseudocode as follows:

```

P=0 // product
For i = 0 to n-1 do
  if  $b_i=1$ 
    P=P+A
  Endif
  Left-shift A
Endfor
  
```

Draw the ASM chart of this shift-and-add multiplier.
 Design the datapath
 Design the control path using JK-FFs

Q.5. **Shift and subtract divider:** Given two n -bit unsigned numbers A and B , we wish to design a digital system that produces two n -bit outputs Q and R , where Q is the quotient of A/B and R is the remainder.

A method that imitates manual computation is as follows: shift the digits in A to the left, one digit at a time, into a shift register R. After each shift operation compare contents of R with B. If $R \geq B$, shift a 1 into Q, otherwise, shift a 0 into Q. A pseudocode describing this method is given below:

```

R=0
For i=0 to n-1 do
    Left-shift R | A          // R | A is the 2n-bit register of R (on the left) and A (on the right)
    if R >= B
        Qi = 1
        R=R-B
    Else
        Qi=0
    Endif
Endfor

```

Draw the ASM chart of this Shift and Subtract Divider
 Design the datapath
 Design the control path using DFF + DEC.

Q.6. A synchronous sequential circuit contains three n-bit registers R1, R2, and R3. In state S0 these registers are loaded with contents InR1, InR2, InR3, respectively. This circuit will be designed to carry out the following register operations: $R1 \leftarrow R3-R2$, $R2 \leftarrow R3-R1$.

Draw the ASM chart of this Shift and Subtract Divider
 Design the datapath
 Design the control path using MUX+DFF+DEC.

Q.7. A synchronous sequential circuit contains two n-bit registers A and B. In state S0 these registers are loaded with contents InA and InB, respectively. This circuit will be designed to carry out the following register operations: if $A \geq B$ then $A=A-B$, else $A=B-A$.

Draw the ASM chart of this Shift and Subtract Divider
 Design the datapath
 Design the control path using JKFFs

Q.8. Design a digital circuit that will compute the 2's complement of the contents of an n-bit register X.

Draw the ASM chart of this Shift and Subtract Divider
 Design the datapath
 Design the control path using JKFFs

Q.9. Design a digital circuit that will compute the absolute value of the contents of an n-bit register X using the signed 2's complement representation..

Draw the ASM chart of this Shift and Subtract Divider

Design the datapath

Design the control path using JKFFs

Q.10. Design a digital circuit that will compute the difference between the number of 1's and the number of 0's within the contents of an n-bit Register X.

Draw the ASM chart of this Shift and Subtract Divider

Design the datapath

Design the control path using JKFFs

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