EASTERN MEDITERRANEAN UNIVERSITY
SCHOOL OF COMPUTING AND TECHNOLOGY
DEPARTMENT OF INFORMATION TECHNOLOGY
COURSE POLICY SHEET

Course Code	ITEC259	**Course Title**	Digital Logic Design
Semester	2020-2021 Fall	**Language**	English
Category	AC (Area Core)	**Level**	Second Year
Workload	180 Hours	**Teaching Format**	3 Hours Lecture, 2 Hours Laboratory
EMU Credit	(3,2,0) 4	**ECTS Credit**	6
Prerequisite(s)	-	**Course Web**	http://staff.emu.edu.tr/ahmetrizaner/en/teaching

Instructors	Prof. Dr. Ahmet Rizaner		
e-mail	ahmet.rizaner@emu.edu.tr	**Office No:**	CT112

Course Description

Digital logic design is concerned with the design of digital electronic circuits which are employed in the design and the construction of the systems such as digital computers and many other applications that require digital hardware. The course presents the basic tools for design of digital circuits and provides the fundamental concepts used in the design of digital systems.

General Learning Outcomes

On successful completion of this course students should be able to:

- Practice arithmetic computations in binary numbering system.
- Explain the basic operations and theorems of Boolean algebra.
- Apply rules of Boolean algebra to simplify Boolean expressions.
- Explain how to translate Boolean expressions into equivalent truth tables and logic gate implementations.
- Explain the fundamentals of logic design from the gate up to the system level.
- Design efficient combinational and sequential logic circuit implementations from functional description of digital systems.
- Practice simple simulations to verify the operation of logic circuits.

Teaching Methodology / Classroom Procedures

- Each week there are three lecture sessions, and two lab sessions.
- Laboratory sessions are organized in parallel to theoretical study given in classrooms.
- During the laboratory sessions, particular aspects of the Digital Logic Design are demonstrated. Students perform different experiments and submit reports for evaluation each week.
- Students are encouraged to use internet to search for various related topics. Lecture notes, assignments, and announcements will be posted on the course's web site.
- There are five online quizzes. The dates of the quizzes will be announced during the lecture hours.
    - Quiz 1 includes Binary Systems topic
    - Quiz 2 includes Boolean Algebra and Logic Gates topic
    - Quiz 3 includes Gate-Level Minimization topic
    - Quiz 4 includes Combinational Logic topic
    - Quiz 5 includes Synchronous Sequential Logic topic
- The duration of the quizzes is 45 minutes.
- There is an online midterm exam which covers Binary Systems, Boolean Algebra, Logic Gates and Gate-Level Minimization topics.
- There is an online final exam which includes Combinational Logic and Synchronous Sequential Logic topics.
- There is no term project.
- Class attendance is compulsory.
- The student is responsible to check the course web site and regularly and view the latest announcements.

Course Materials / Main References
Text Book: M. M. Mano and M. D. Ciletti, Digital Design, 5th Ed., Prentice-Hall, 2013, ISBN-13: 978-0-13-277420-8. ***Resource Books:*** 1. M.M. Mano and C. R. Kime, Logic and Computer Design Fundamentals, 5h Ed. Prentice-Hall, 2015, ISBN-13: 978-0133760637. 2. J. F. Wakerly, Digital Design Principles and Practice, 4rd Ed., Prentice-Hall, 2005, ISBN-13: 978-0131863897. ***Lecture Notes:*** All course materials are also available online in Adobe PDF (Portable Document Format).

Weekly Schedule / Summary of Topics	
Weeks 1-2	**Binary Systems:** Digital Systems. Binary Numbers. Number Base Conversions. Octal and Hexadecimal Numbers. Complements. Signed Binary Numbers. Binary Codes. Binary Storage and Registers. Binary Logic.
Weeks 3-4	**Boolean Algebra and Logic Gates:** Basic Definitions. Axiomatic Definition of Boolean Algebra. Basic Theorems and Properties of Boolean Algebra. Boolean Functions. Canonical and Standard Forms. Other Logic Operations. Digital Logic Gates.
Weeks 5-7	**Gate-Level Minimization:** The Map Method. Four-Variable Map. Five-Variable Map. Product of Sums Simplification. Don't-Care Conditions. NAND and NOR Implementation. Exclusive-OR Function.
Weeks 8-9	**Midterm Examinations Period**
Weeks 10-12	**Combinational Logic:** Combinational Circuits. Analysis Procedure. Design Procedure. Binary Adder-Subtractor. Decimal Adder. Binary Multiplier. Magnitude Comparator. Decoders. Encoders. Multiplexers.
Weeks 13-15	**Synchronous Sequential Logic:** Sequential Circuits. Latches. Flip-Flops. Analysis of Clocked Sequential Circuits. State Reduction and Assignment. Design Procedure.
Weeks 16-17	**Final Examinations Periods**

Requirements
▪ Each student can have only one make-up exam. One who misses an exam should provide a medical report or a valid excuse within 3 days after the missed exam. The make-up exam will be done at the end of the term and will cover all the topics. No make-up exam will be given for the quizzes. ▪ Students who do not pass the course and fail to attend the lectures regularly may be given NG grade. ▪ Instructions for the submission of assignments, online quizzes and exams will be posted on the course website. It is each student's responsibility to read and follow the instructions. Failure to follow the submission instructions may result in the assignment receiving a mark of zero.

Method of Assessment				
Evaluation and Grading	**Quizzes**	**Lab**	**Midterm Exam**	**Final Exam**
Percentage	25 %	15 %	25 %	35 %