CMPE 226 Electronics Lab Report
Experiment # 7 Transistor Familiarization & Common-Emitter Transistor Circuit

Partners

	Std. No	Name	Group
1.	_____	_____	_____
2.	_____	_____	_____
3.	_____	_____	_____

Date _____

Objectives:

1) *Ability to recognize transistors in various physical forms.*
2) *Understanding of the basic construction of PNP and NPN* transistors
3) *Understanding of junction biasing and the direction and magnitude of current flows*
4) *To familiarize with common emitter output collector characteristics*

Introduction

Transistors are three-terminal devices constructed in the form of two semiconductor junctions, rather like two junction diodes. Fig. 1 shows the two types NPN, and PNP, governed by the physical arrangement of the P- and N- type semiconductors materials

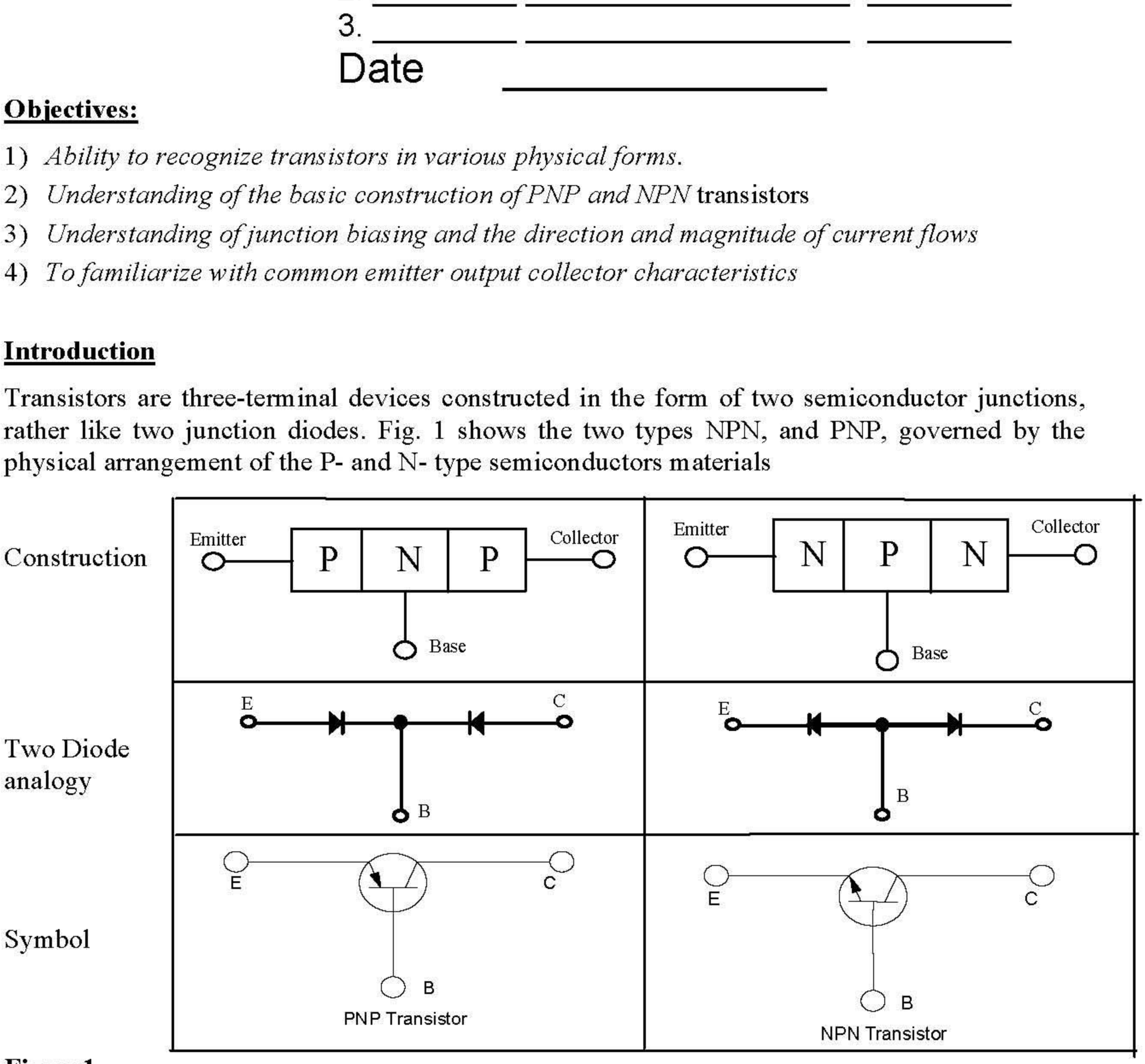

Figure1
Two types of Transistor

Each of the PN Junctions in this diagram behaves individually like the simple diode you studied in Experiment 2, but when joined together in this way, the behavior is very different.

EX_3.1 Measurement of Transistor Currents

Construct transistor circuit as below

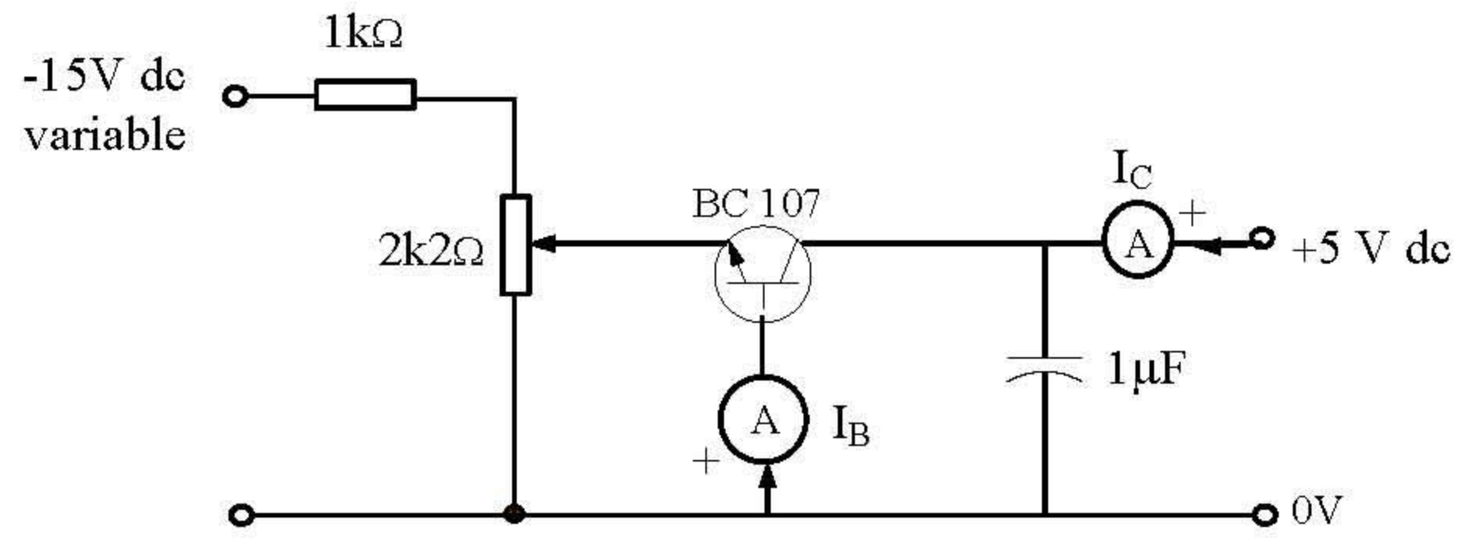

Fig. 2Transistor Test Circuit

- The capacitor is provided to ensure that the circuit is stable and has no effect on your measurements

EXPERIMENTAL PROCEDURE

1) Turn the potentiometer to zero (anti-clockwise) and switch on both power supplies.

2) Increase voltage from potentiometer so that I_C approximately equals 6mA and record the values of I_C and I_B in the **table 1**

3) Again increase voltage from potentiometer until I_C approximately equals 10mA; again record I_C and I_B in **table 1**.

I_C	I_B (μA)	$\beta=I_C/I_B$	$I_E=I_C+I_B$(mA)	$\alpha=I_C/I_E$

Table 1

Q1) Did your readings of V_{EB} confirm that the forward-biased E-B junction is acting like a simple diode? Explain.

Q2) Dou your results show that α and β

a) Increase

b) Decrease, or;

c) Stay constant as I_C increases

EX_3.2 To find I_C is controlled by I_B and V_{CE}

- Construct the circuit like in Figure 3

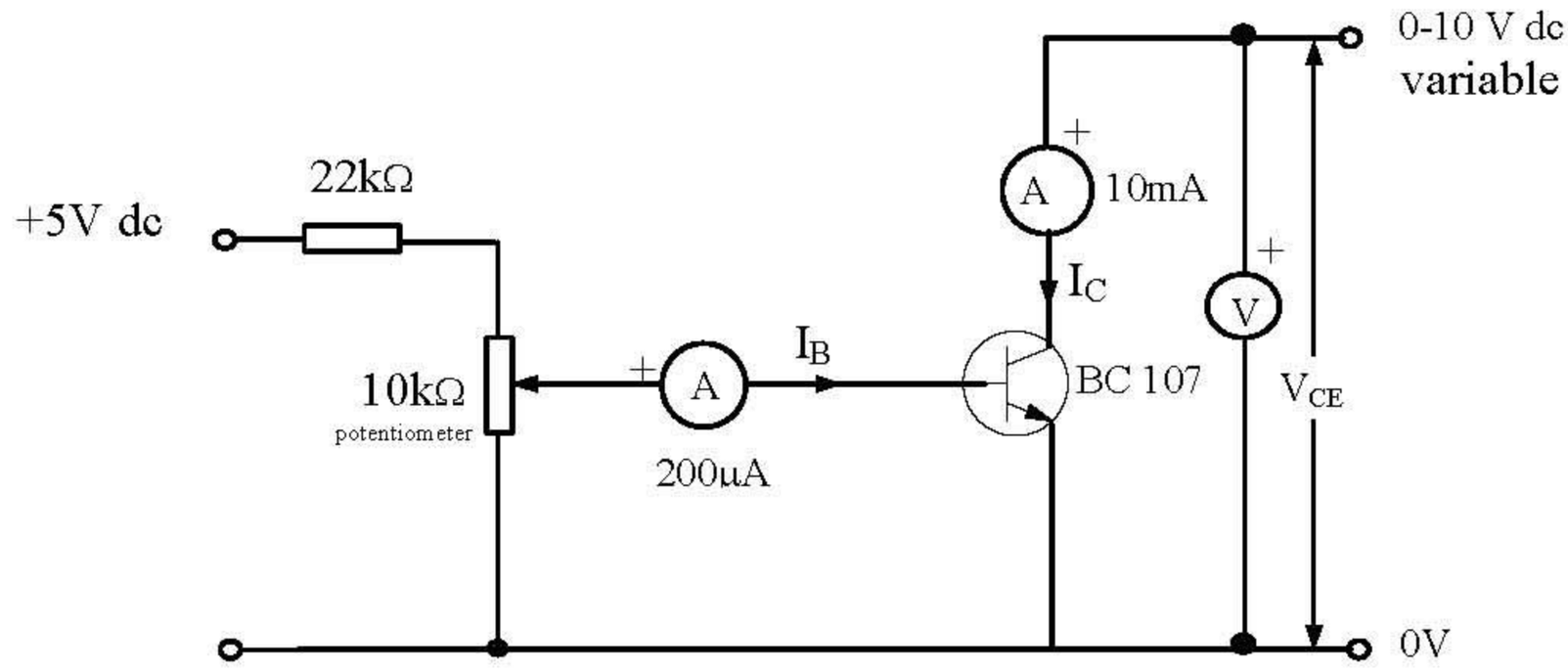

Fig. 3 Test Circuit

- Copy the results as in table 2 and prepare a graph as shown in Fig 4

- Set V_{CE} 1V then use the potentiometer to adjust I_B to each value given in the Table2
- At each setting record I_C in the appropriate column. Then repeat for each other V_{CE} value
- Plot I_C against V_{CE} for each value of I_B on your graph
- The graphs you now have are the 'output' or 'collector' characteristics

I_B	I_C (mA) for V_{CE} = ……(V)			
µA	V_{CE}=1V	V_{CE}=2V	V_{CE}=5	V_{CE}=10
10				
20				
30				
40				
50				

Table 2 Results for I_C

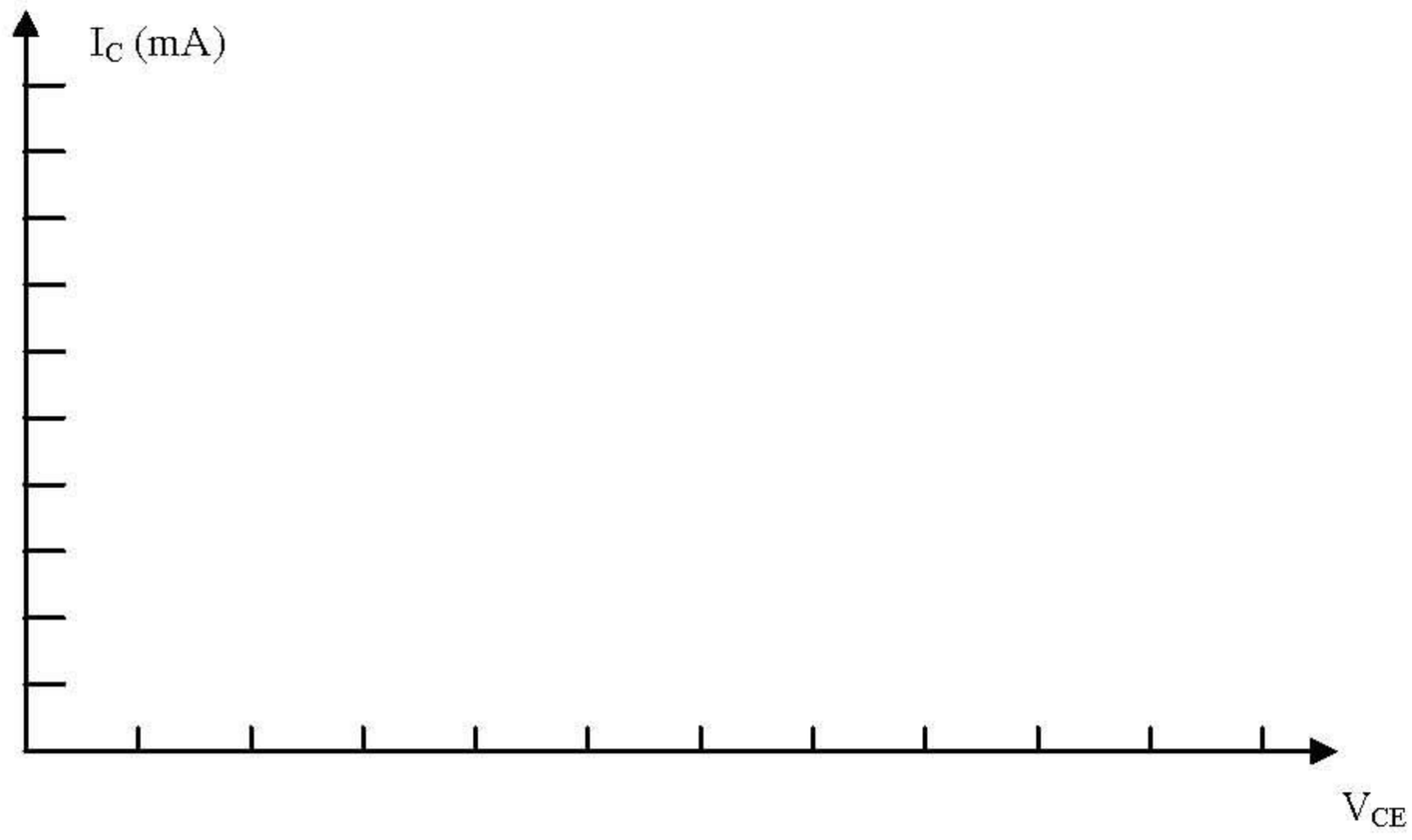

Figure 4
BC107
Collector
Characteristics

Q3) What happens to I_C when V_{CE} becomes less than 0.6V?

Q4) What do you notice about the effect of V_{CE} upon I_C?

EX_3.3 Constructing a Load Line

Figure 5 shows a circuit in which the collector bias is applied through a load resistor. V_{CC} is the term used for the bias voltage to distinguish it from V_{CE} because when a current I_C is flowing these two will be different

By Ohm's Law: $V_{CE}=V_{CC}-I_CR$

Therefore when $I_C=0$, $V_{CE}=V_{CC}$

And when $V_{CE}=0$, $I_C=V_{CC}/R$

- Now on your graph (**Figure 4**) plot these two points V_{CE} and I_C for

$\underline{I_C=0}$, $\underline{R=1\ k\Omega \text{ and } V_{CC}=+10V}$

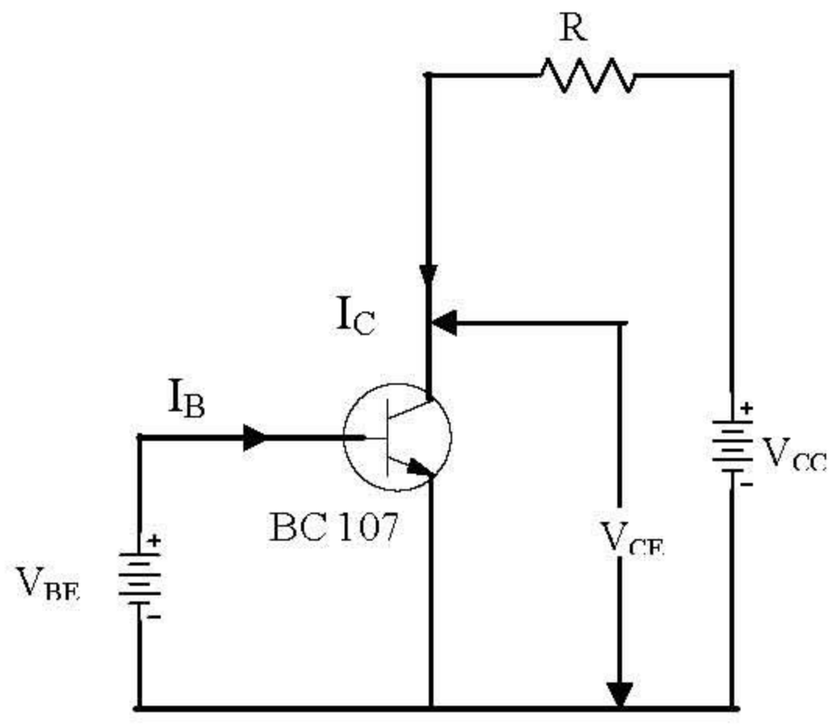

Fig. 5 Addition of Load Resistor

CONCLUSIONS: