CMPE223- Digital Logic Design

Department: Computer Engineering

Instructor information
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Meeting times and places
Tuesday: 10:30-12:20, Room CMPE Amphi
Wednesday: 08:30-10:20, Room CMPE Amphi
Thursday: 16:30-18:20, Room LLAB (Lab)

Program Name: Computer Engineering	**Program Code:** 25	
Course Number: CMPE223	**Credits:** 4 Cr	**Year/Semester:** 2021-2022 Fall

☒ Required Course ☐ Elective Course

Prerequisite(s):
MATH163 Discrete Mathematics

Catalog description:
Binary Systems (Binary Numbers, Octal and Hexadecimal Numbers, Number Base Conversions, Complements, Signed Binary Numbers, Binary Codes, Binary Logic). Boolean Algebra and Logic Gates (Basic Definitions, Basic Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms. Simplification of Boolean Functions (The Map Method), Two- Three- and Four-Variable Maps, Product of Sums Simplification, NAND and NOR Implementation, Other Two-Level Implementations, Don't-Care Condition. Combinational Logic (Design Procedure, Adders, Subtractors, Code Conversion, Analysis Procedure, Multilevel NAND Circuits, Multilevel NOR Circuits, Exclusive-OR Functions). MSI Components (Binary Adder and Subtractor, Decimal Adder, Decoders and Encoders, Multiplexers). Synchronous Sequential Logic, Flip-Flops, Analysis of Clocked Sequential Circuits. Design of Clocked Sequential Circuits: Design Procedure, State Reduction, State Assignment and FF Excitation Tables.

Course web page:
http://cmpe.emu.edu.tr/courses/cmpe223 or https://staff.emu.edu.tr/muhammedsalamah/en/teaching/cmpe223

Textbook(s):
J. F. Wakerly, "*Digital Design: Principles and Practices*", Prentice-Hall, 2006.

Indicative basic reading list :
1. S. Brown and Z. Vranesic, "Fundamentals of Digital Logic with VHDL Design", McGraw-Hill, 2009
2. Richard S. Sandige, "*Digital Design Essentials*," Prentice-Hall 2002.

Topics covered and class schedule (tentative):
(4 hours of lectures per week)

Week 1, 2	Binary, Octal, and Hexadecimal Numbers, Number Base Conversions, Signed Binary Numbers and Complements, Binary Addition, Subtraction, and Overflow, Binary Codes, and Binary Logic.
Weeks 3-4	Simplification of Boolean Functions, SOP and POS Simplifications, NAND and NOR Implementations, Multilevel NAND and NOR Circuits, Exclusive-OR Functions, Don't-Care Conditions.
Weeks 5,6	Combinational Logic, Analysis Procedure, Design Procedure, Adders/Subtractors, Code Conversion, and Python-based Implementations
Weeks 7,8	MSI Components, Binary Adder and Subtractor, Decimal Adder,
Weeks 9,10	Midterm
Weeks 11,12	Decoders and Encoders, Multiplexers,
Weeks 12,15	Synchronous Sequential Logic, Flip-Flops, Analysis of Clocked Sequential Circuits. Design of Clocked Sequential Circuits: Design Procedure, State Reduction, State Assignment and FF Excitation Tables
Weeks 17-18	Finals

Laboratory schedule (tentative):
(2 hours of laboratory per week)

Week 1, 2	Lab preparations and groups arrangements.
Week 3	Getting familiar with the tools
Week 4	Introduction to Quartus II Design Environment.
Week 5	Introduction to Hardware Description using VHDL Programming Language.
Week 6	Basic VHDL Prog. of Combinational Circuits
Week 7	Basic VHDL Prog. of Combinational Circuits
Week 8,9	Midterm
Week 11	Basic VHDL Prog. of Combinational Circuits
Week 12	Basic VHDL Prog. of Sequential Circuits
Week 13	Basic VHDL Prog. of Sequential Circuits
Week 14	No Lab

Course learning outcomes:
Upon successful completion of the course, students are expected to have the following competencies:
1. Perform the mathematical operations using signed and unsigned binary numbers (1)
2. Use algebraic manipulations associated with Boolean variables to build and evaluate Boolean expressions and functions (1)
3. Use the Karnaugh map technique to simplify Boolean functions (SOP/POS) with/without don't care conditions (2)
4. Design combinational logic circuits using AND, NOT, OR, NOR, NAND, XOR and XNOR logic gates (2)
5. Analyze combinational circuits and find their functions (2)
6. Use functional combinational units such as adders/subtractors, comparators, decoders, multiplexers, to design larger size combinational logic systems (2)
7. Analyze sequential logic circuits by constructing the state tables / state diagrams and find their functions (1)
8. Design sequential logic circuits using state diagrams, state tables, and Flip-Flop excitation tables (2)
9. Construct initial state transition diagrams, perform state reduction and assignment from the verbal description of the circuit behavior (2)
10. Simulate the behavior of combinational and sequential circuits using Python Programming language (6)

	Method	**No**	**Percentage**
Assessment (tentative)	Midterm Exam	1	30%
	Final Examination	1	50%
	Assignment	5	5%
	Lab	~6	15%

Policy on makeup: There is no makeup for the quizzes. Only one makeup exam can be given for one of the missed exams (midterm or final) according to the University regulations. In order to be able to enter a makeup exam, you MUST submit a written report to your instructor stating your excuse within 3 days of that examination.

Policy on cheating and plagiarism: Any student caught cheating at the exams or assignments will automatically fail the course and may be sent to the disciplinary committee at the discretion of the instructor.

Policy on NG grades: NG grade will be given in the following cases:
Lab attendance < 50% or
Missing both Midterm and Final Exams.

Contribution of course to ABET criterion 5
Credit Hours for:
Mathematics & Basic Science : 0
Engineering Sciences and Design : 4
General Education : 0

Relationship of the course to program outcomes
The course has been designed to contribute to the following program outcomes:
1) an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.
2) an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors
6) an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.

Prepared by: Assoc. Prof. Dr. Muhammed Salamah	**Date Prepared:** Oct. 12, 2021