EASTERN MEDITERRANEAN UNIVERSITY
COMPUTER ENGINEERING DEPARTMENT
CMPE 223 DIGITAL LOGIC SYSTEMS

EXPERIMENT $^\vee$ *: INTRODUCTION TO QUARTUS II SOFTWARE : LET'S*
   *REVIEW OUR MIND*

Objectives:
This laboratory work aims to review the subjects covered in the previous three experiments and make practice using our combined knowledge gained over these laboratory works. So far, we have covered the schematic entry and simulation of combinational circuits and the implementation of Boolean functions given in truth table form. The experimental steps described below will lead you to make practice over these subjects.

Preliminary Work:
Perform the Experimental Work.

Experimental Work:

E1. You are given the description of a combinational circuit with four inputs and three outputs that implements a 4-bit comparator. It checks for its two 2-bit input binary numbers $A=a_1a_0$ and $B=b_1b_0$, either A=B, or A>B, or A<B. The output E=1 if A=B, the output G=1 if A>B, and the output L=1 if A<B. Enter the schematic description of the 4-bit binary comparator circuit, compile, and simulate it to verify its correct operation. (**Note that; you must have 4 inputs and three outputs in your waveform editor**)
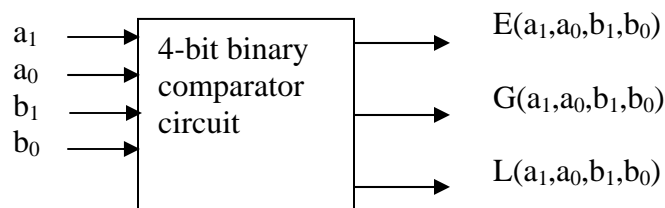

Expressions of output Boolean functions are:

$E(a_1,a_0,b_1,b_0)=(a_1 \odot b_1). (a_0 \odot b_0)$

$G(a_1,a_0,b_1,b_0)=(a_1.b_1{}').+(a_1 \odot b_1).(a_0.b_0{}')$

$L(a_1,a_0,b_1,b_0)=(a_1{}'.b_1)+ (a_1 \odot b_1).(a_0{}'.b_0)$

E2. Consider the following truth table description of a combinational circuit that functions as a 7-segment LED display driver. That is, when a 4-bit BCD is applied to the circuits, its outputs identify the LED segments that will shine to display the corresponding decimal digit. Find the equations of a, b, c, …., d using the truth table below; then draw the circuit of 7-segment LED display driver and simulate the below truth table description in QUARTUS II software. (**Note that; you must have 4 inputs and 7 outputs in your waveform editor**)
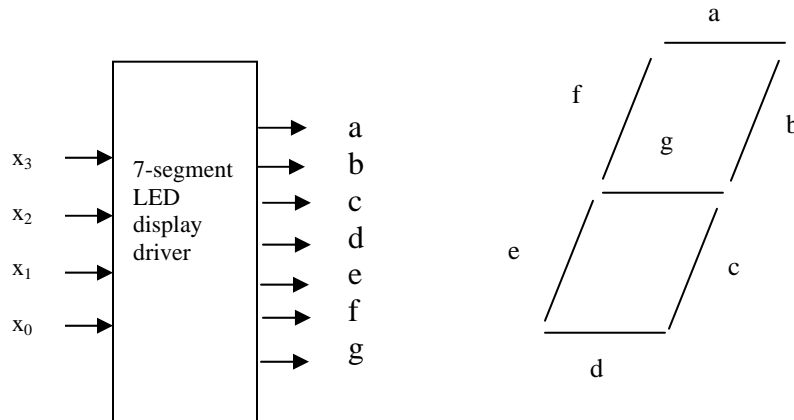
| BCD Inpt				7-segment functions						
x_3	x_2	x_1	x_0	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1

NOTES:

1. You should come to the laboratory with well-prepared preliminary work.
2. Your preliminary work must be prepared by yourself, it is encouraged to exchange ideas with your friends, but the final work done must be of your own.

Good Luck

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Sample VHDL code:
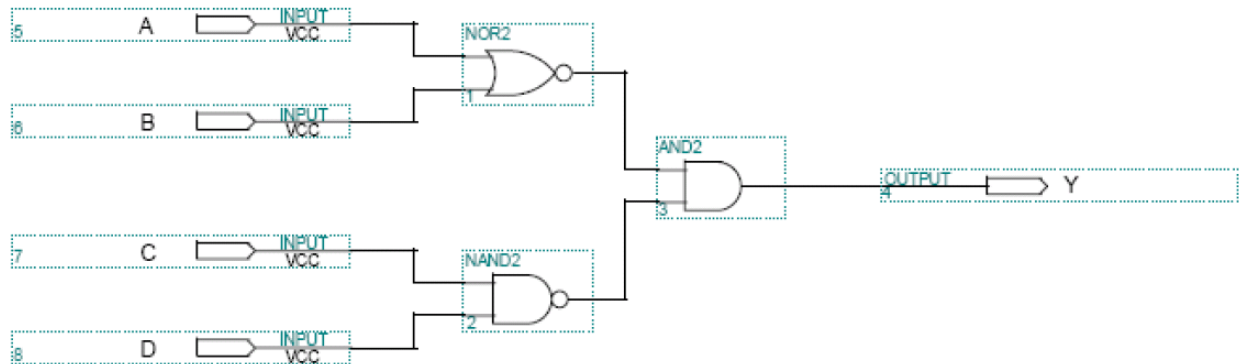

```
library ieee;
use ieee.std_logic_1164.all;

entity MyTestCircuit is

port( a,b,c,d: in std_logic;
            y: out std_logic);
end MyTestCircuit;

architecture Flow of MyTestCircuit is
signal s1,s2: std_logic;

begin
  s1 <= a nor b;
  s2 <= c nand d;
  y <= s1 and s2;
end Flow;
```