12 April, 2019

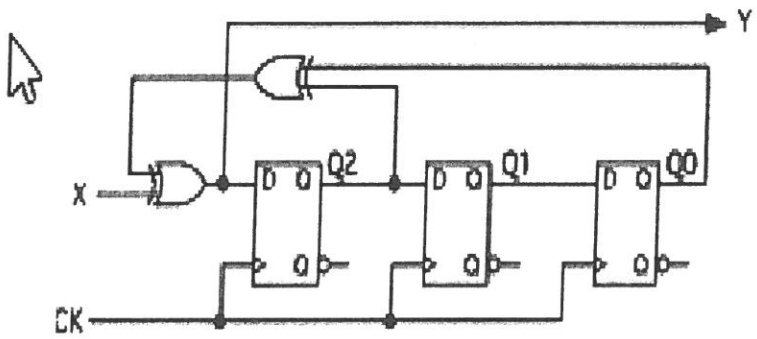
EMU – COMPUTER ENGINEERING DEPARTMENT
CMPE224 DIGITAL LOGIC SYSTEMS
FIRST MIDTERM EXAMINATION

Name & Surname: Adnan Acan **Std. ID:**

Duration:105 Minutes Solutions

Exam is over 100 and all questions have equal weight.

Q.1. Given the following synchronous sequential circuit, analyse it draw the state transition diagram (graph).



Q.2. Design a 4-bit multifunction register/counter that is controlled by two control inputs S1 ve S0 as follows:

S1	S0	Function Mode
0	0	Parallel Load
0	1	Up counter
1	0	Shift right
1	1	Negate the contents

Design this multifunction register/counter using JK-FFs

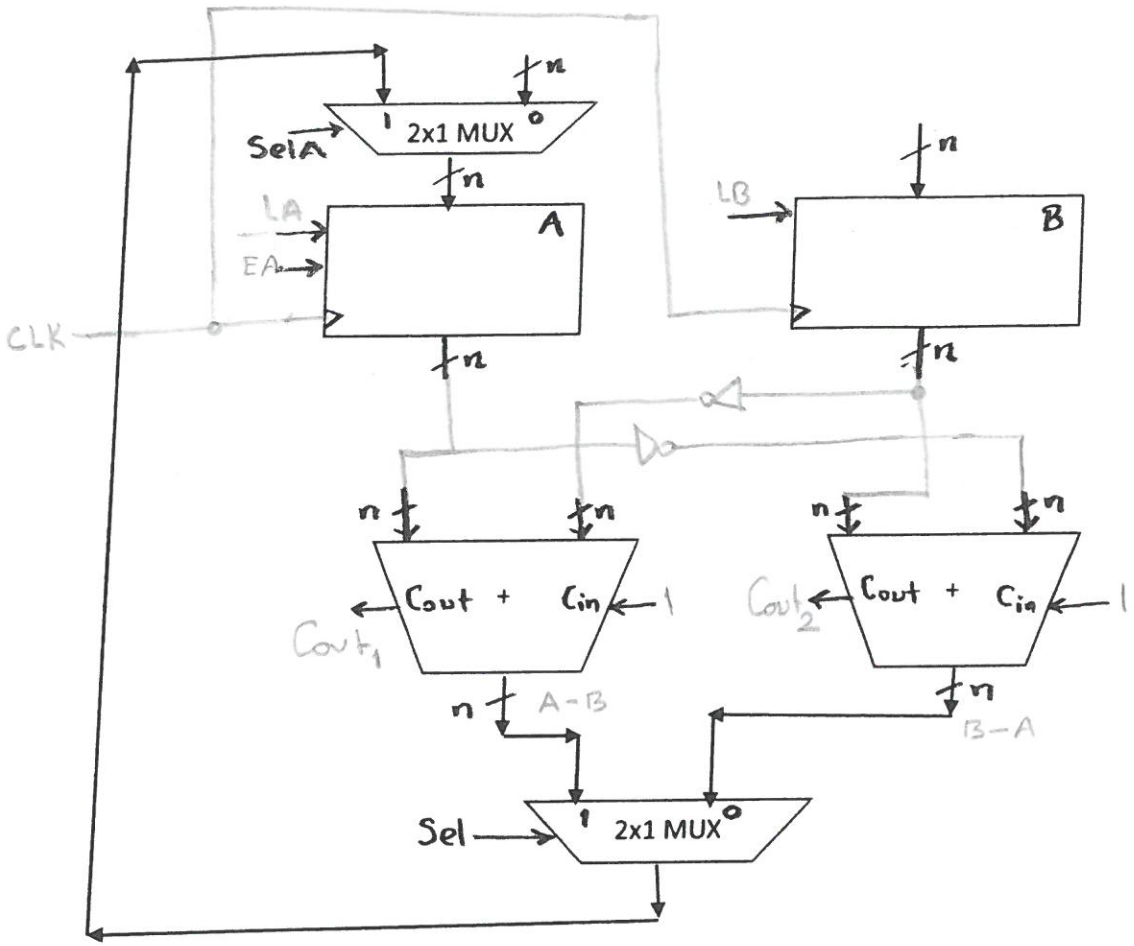
Q.3. Design a synchronous sequential circuit with two inputs, A and B, and a single output Y. The circuit is required to compare the previous value of A with the present values of A and B at every clock cycle and make the output Y=1 if the previous value of A is 1 and at least one of A or B has value a present value of 1 at the current clock cycle.

a) Draw the state transition diagram of the described circuit.

b) Write down the state transition table of the circuit.

c) Implement using JK-FFs.

Datapath:



$LA = S_1' S_0 + S_2 + S_3$

$LB = S_1' S_0$

$Sel\,A = S_2 + S_3$

$EA = S_1' S_0 + S_2 + S_3$

$Sel = Cout_1$

ASM : 6

Datapath : 9

Control : 10

CMPE 224/BLGM224
midterm Exam solutions

Q.1. $D_0 = Q_1$, $D_1 = Q_2$, $D_2 = X \oplus Q_2 \oplus Q_0$, $Y = X \oplus Q_2 \oplus Q_0$

X	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	Y
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	1	0	1	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	0	0
0	1	1	0	1	1	1	1
0	1	1	1	0	1	1	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	1	0	1	1
1	0	1	1	0	0	1	0
1	1	0	0	0	1	0	0
1	1	0	1	1	1	0	1
1	1	1	0	0	1	1	0
1	1	1	1	1	1	1	1

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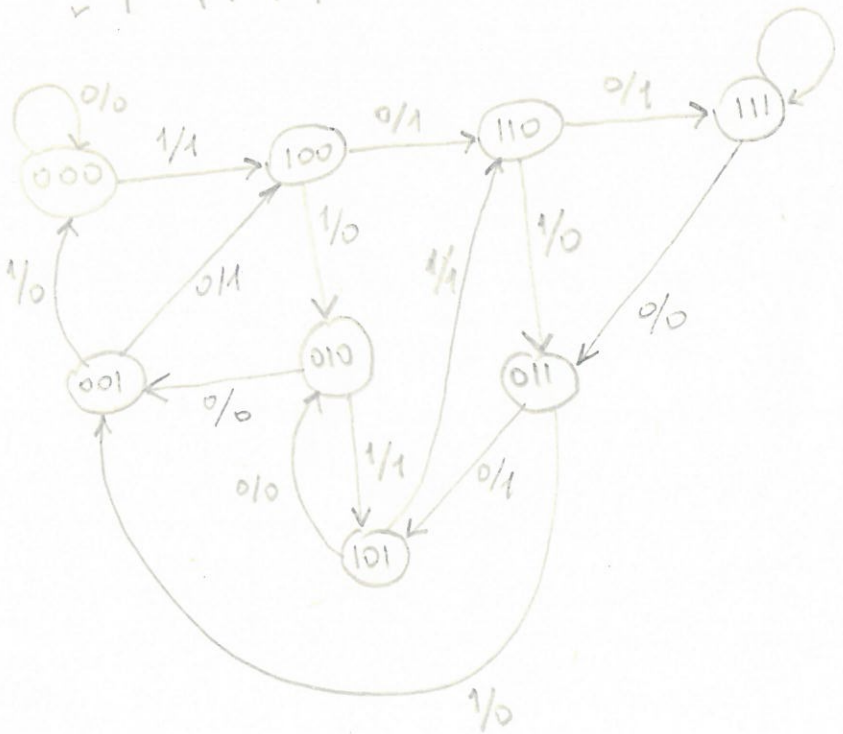

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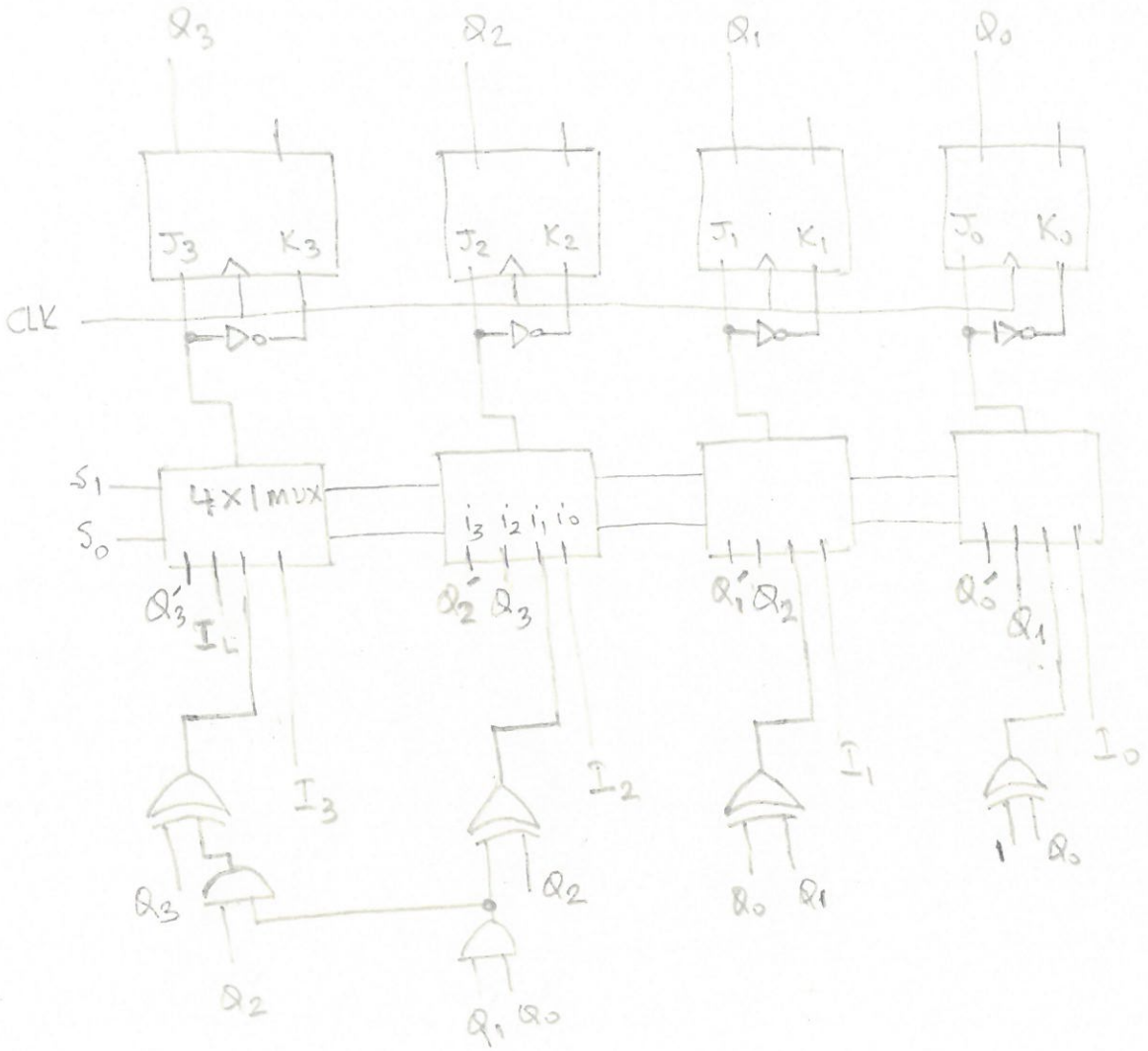
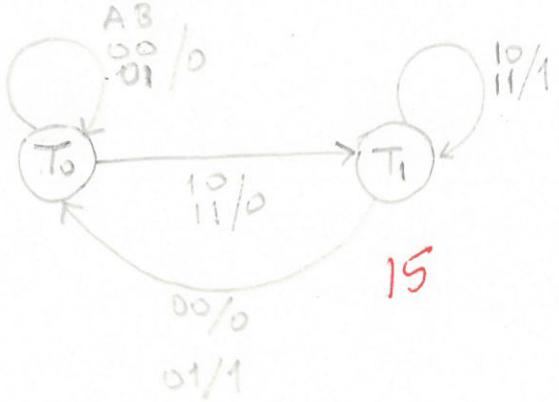
Q.2.


Q3
Q2
Q1
Q0
J3
K3
J2
K2
J1
K1
J0
K0
CLK
S1
S0
4x1 MUX
i3 i2 i1 i0
Q3'
I1
Q2' Q3
Q1' Q2
Q0'
Q1
I3
I2
I1
I0
Q3
Q2
Q0
Q1
1
Q2
Q1 Q0

Q.3.



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A	B	Q	Q^+	Y
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	1	1

$Q^+ =$

A \ B			1	
			1	
	1	1		

Q

$Q^+ = A$

$= A \cdot Q + A \cdot Q'$

J K'

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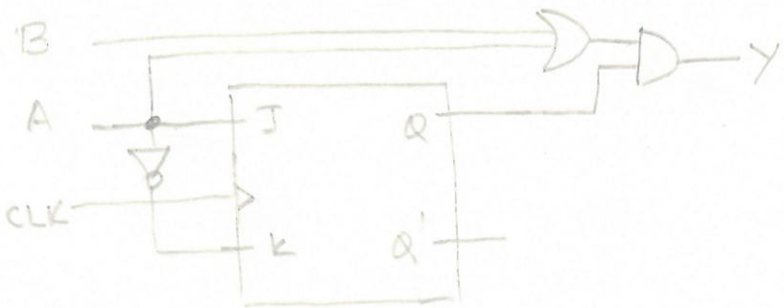
$Y =$

A \ B			1	
	1	1		

Q

$Y = AQ + B \cdot Q$

$= (A+B) \cdot Q$



Q.4.

Datapath (on The Paper)

Controlpath

PS $Q_1 Q_0$	inputs S	$Cout_1$	NS $Q_1^+ Q_0^+$	Output S_0	S_1	S_2	S_3
0 0	0	x	0 0	1	0	0	0
0 0	1	x	0 1	1	0	0	0
0 1	x	1	1 1	0	1	0	0
0 1	x	0	1 0	0	1	0	0
1 0	x	x	0 0	0	0	1	0
1 1	x	x	0 0	0	0	0	1