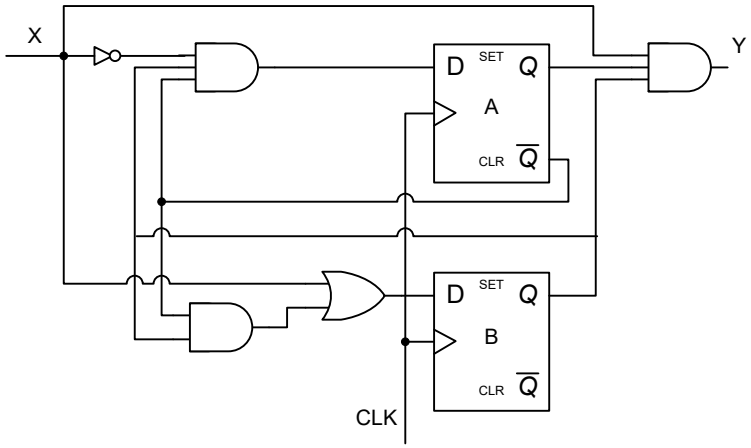
EMU-COMPUTER ENGINEERING DEPARTMENT
CMPE224 DIGITAL LOGIC SYSTEMS
EXERCISE QUESTIONS IV

Q.1. **Consider the following synchronous sequential circuit**

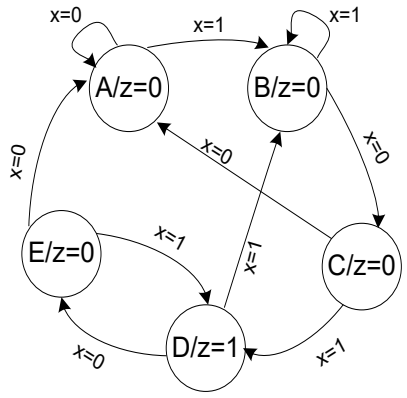


a) Is this a **Moore or Mealy** machine?

b) What are the **next-state** and **output equations** for this machine?

c) Analyze and draw a **state transition diagram** for the machine **showing all possible states** and **all possible transitions.**

Q.2. **Consider the following state transition diagram of a synchronous sequential circuit.**



a) Construct the **state transition table** for this diagram

b) **Minimize the number of states** by eliminating any redundant states, if possible showing all intermediate steps and

c) also show final result as a **state transition diagram graph**

Q.3. Design a synchronous sequential circuit with one input X and two outputs C and S such that the circuit will compute the sum and carry ouputs of the last two bits on the single input line X and assign the sum bit of addition to S and carry bit of addition to C. Overlapping of bits over the last two values of X is **allowed**. Carry out the design starting from the initial state transition diagram (table) to end using JK-FFs.

Q.4. A serial two's complementer is to be designed. This clocked sequential circuit has two inputs X and Y and one output Z. A binary integer of arbitrary length is presented to the circuit on input X; LSB appears first. When a given bit is presented on input X, the corresponding output bit appears on Z during the same clock cycle. To indicate that a sequence is complete and that the circuit is to be initialized to receive another sequence, input Y is set to 1. Y is zero otherwise. [Hint: use the shortcut method of taking 2's complement].

a) Find the initial and the minimal state transition tables.

b) Make a state assignment.

c) Design the circuit using D FFs.

Q.5. Design a synchronous sequential circuit with two inputs, A and B, and a single output Y. The circuit is required to compare the previous value of A with the present values of A and B at every clock cycle and make the output Y=1 if the previous value of A is 1 and at least one of A or B has value a present value of 1 at the current clock cycle.

a) Draw the state transition diagram of the described circuit.

b) Write down the state transition table of the circuit.

c) Implement using JKFFs.

Q.6. Design a 3-bit counter-like circuit controlled by an input w. If w=1, then the counter adds 2 to its contents, wrapping around 8 or 9. Thus, if the present state is 8 or 9, then the next state becomes 0 or 1, respectively. If w=0, then the counter subtracts 1 from its contents, acting as a normal down counter. Use RS-FFs in your design.

Q.7. We wish to design a sequence detector circuit, which detects three or more consecutive 1's in a string of bits coming through an input line X.

(a) Find the MOORE-TYPE state transition diagram.

(b) Determine the state transition table

(c) Implement the circuit using D flip-flops.

In case of any questions, do not hesitate to ask!

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