**EASTERN MEDITERRANEAN UNIVERSITY**

**DEPARTMENT OF COMPUTER ENGINEERING**

**CMPE223 NUMERICAL LOGIC SYSTEMS**

**Experiment 7: Verilog language, Latch, D-FF, T-FF, JK-FF**

**Simple SR-Latch:**



**SR-Latch Verilog code:**

module SR\_LATCH(S, R, Q, Qbar);

 input S, R;

 output Q, Qbar;

 reg Q, Qbar;

 always @(S, R, Q, Qbar)

 begin

 Q <= !(R | Qbar);

 Qbar <= !(S | Q);

 end

endmodule

**Simple D-FF:**

The D-FF is a simple bit memory that is connected to the clock signal.

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**D-FF code:**

module D\_FF(D, clk, Q);

 input D, clk;

 output Q;

 reg Q;

 always @(posedge clk)

 begin

 Q <= D;

 end

endmodule

**Simple T-FF:**

T-Flip Flop is toggle FF.



**T-FF Code:**

module T\_FF(T, clk, Q, Qbar);

 input T, clk;

 output Q, Qbar;

 reg Q, Qbar;

 reg S, R;

 always @(posedge clk)

 begin

 R <= T & clk & Q;

 S <= T & clk & Qbar;

 Q <= !(Qbar | R);

 Qbar <= !(Q | S);

 end

endmodule

**JK-Flip Flop:**

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**JK-FF Code:**

module JK\_FF(J, K, clk, Q, Qbar);

 input J, K, clk;

 output Q, Qbar;

 reg Q, Qbar;

 reg S, R;

 always @(clk)

 begin

 S <= !(Qbar & clk & J);

 R <= !(Q & clk & K);

 Q <= !(S & Qbar);

 Qbar <= !(R & Q);

 end

endmodule

**T-FF Counter:**

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**T-FF Counter Code:**

module Counter(T, clk, Q, Qbar);

 input T, clk;

 output [3 : 0] Q, Qbar;

 T\_FF t0(T, clk, Q[0], Qbar[0]);

 T\_FF t1(Q[0], clk, Q[1], Qbar[1]);

 T\_FF t2(Q[1], clk, Q[2], Qbar[2]);

 T\_FF t3(Q[2], clk, Q[3], Qbar[3]);

endmodule

module T\_FF(T, clk, Q, Qbar);

 input T, clk;

 output Q, Qbar;

 reg Q, Qbar;

 reg S, R;

 always @(posedge clk)

 begin

 R <= T & clk & Q;

 S <= T & clk & Qbar;

 Q <= !(Qbar | R);

 Qbar <= !(Q | S);

 end

endmodule

**Ömer DEMİR**