$\qquad$

| Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Total |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |  |  |

Q1) [20pts] Consider the following MIPS code segment. Note: values of a0 and a1 are passed from the calling function and the result is returned in $\mathbf{v 0}$.

```
f1 :
    lw $t0, 0($a0)
    addi $t1, $0, 1
loop:
    bge $t1, $a1, exit
    mul $t2, $t1, 4
    add $t2, $t2, $a0
    lw $t2, 0($t2)
    ble $t2, $t0, next
    add $t0, $t2, $0
next:
    addi $t1, $t1, 1
    j loop
exit:
    add $v0, $t0, $0
    jr $ra
```

a) Translate the function f 1 into a C code [use variable names as register names].
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
$\qquad$
b) Describe briefly what the function f1 perform?

Q2) [6pts] For multi-Cycle CPU, decide which of the following is true or false:
a) $\qquad$ Faster instructions are not held back by slower ones.
b) $\qquad$ We don't have to duplicate any hardware units.
c) $\ldots \ldots \ldots \ldots$ The cycle time is limited by the slowest functional unit.

Q3) [4pts] For a multi-cycle processor, consider the following code segment:
lw \$t2, 0(\$t3)
lw \$t3, 4(\$t3)
beq \$t2, \$t3, Label
add \$t5, \$t2, \$t3
sw \$t5, 8(\$t3)
Label:
a) What is going on during the $8^{\text {th }}$ cycle of execution? $\qquad$
b) In what cycle is the branch target address is calculated? $\qquad$

Q4) [20pts] Assume that the following MIPS program is run on a 500 MHz processor, with a clock cycle time of $\mathbf{2 n s}$. The number of clocks per instruction is shown in the table. Let $\$ \mathbf{1} 1=5$, calculate the total CPU time required for executing this function.

```
func:lw $t0,0($a0)
    addi $t1,$0,1
loop:bge $t1,$a1,exit
    mul $t2,$t1,4
    add $t2,$t2,$a0
    lw $t2,0($t2)
    add $t0,$t2,$0
    addi $t1,$t1,1
    j loop
exit:add $v0,$t0,$0
jr $ra
```

The total number of cycles is $\qquad$
The total CPU time is $\qquad$

Q5) [25pts] Consider the single-cycle data-path shown below. Assume that we wish to add the following new instruction jm (jump memory) to this data-path.

## jm offset(\$rs)

The jm instruction loads a word from effective address (\$rs + offset), this is similar to lw except the loaded word is put in the PC instead of register $\$ \mathbf{r t}$.
a) [10pts] Add any necessary data-path(s) and justify the need for the modification(s).
b) [10pts] High-light the data-path for executing this instruction.

c) [5pts] In the given table below, provide the corresponding control signals to support the $\mathbf{j m}$ instruction.

| RegDst | RegWrite | ALUSrc | ALUOp | MemWrite | MemRead | MemToReg | PCSrc |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |  |  |  |

## MemIndAdd rt,offset(rs)

to the multicycle data-path shown below. This instruction employs the following operations:

```
tmp=memory[offset+rs]
tmp=memory[tmp]
```


## $r t=r t+t m p$

a) [10pts] Add clearly any necessary data-paths and justify the need for the modifications, if any.

b) [10pts] Provide the finite state diagram for executing this instruction. Specify the required control lines values starting from the $3^{\text {rd }}$ step.
Step1: fetch Step2: Decode Step3:.................

c) [5pts] how many cycles required for executing this instruction.

